System level 3D integration and system-in-package for chemical sensing microsystems

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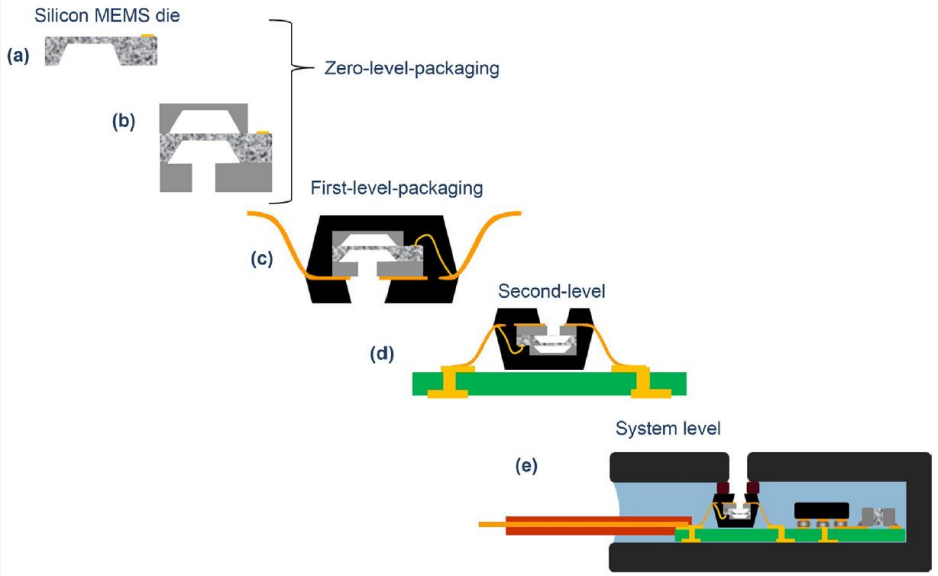
Overview:

- introduction to MEMS packaging and 3D integration
- 3D integration vs. wafer-level integration
- specific cases for chemical and biosensing:
    - Lab-on-chip (Biosensing)
    - Gas-chromatography (Chemical sensing)
- Conclusions

Examples of pecularities in MEMS packaging

Example 1: Pressure sensor:

- Starting from MEMS die
- **Cavity formation (zero-level packaging)**
- First-level packaging: *as usual*
- System-level packaging: **sensor exposure**



Zero-level packaging

Traditional semiconductor packaging distinguishes between first level and second level packaging.

First level refers to assembly, interconnection and encapsulation of the die.

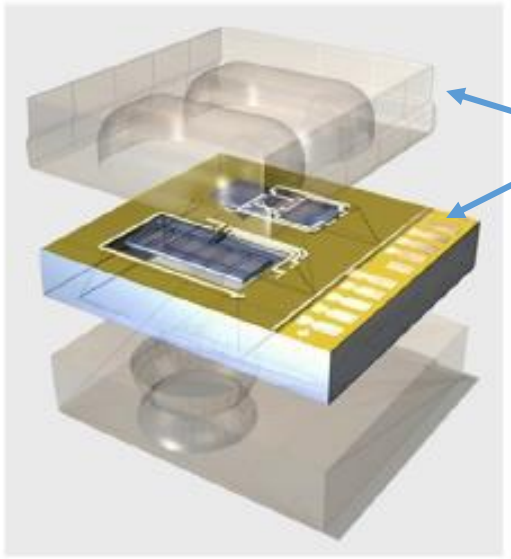
Second level means assembly of the packaged semiconductor onto a printed circuit board (PCB).

→ **In MEMS packaging, the term zero-level packaging is introduced.**

In this example, it refers to the process of cavity creation, necessary for the pressure sensor, and it is typically performed at wafer level (e.g. with wafer bonding techniques).

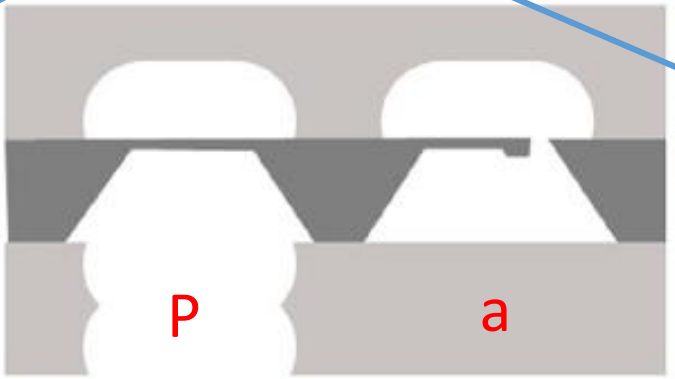
Handbook of Silicon Based MEMS Materials and Technologies. DOI: http://dx.doi.org/10.1016/B978-0-323-29965-7.00037-3

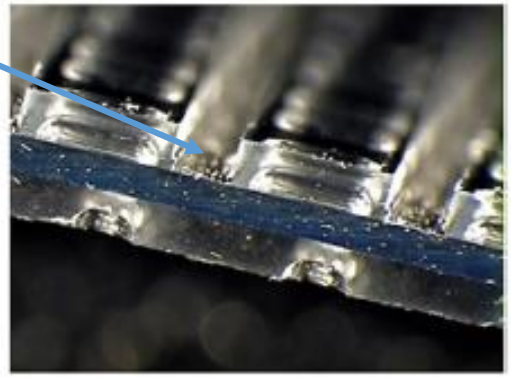
3D integration of MEMS: introduction



…at wafer level?

Infineon integrater pressure and acceleration sensor



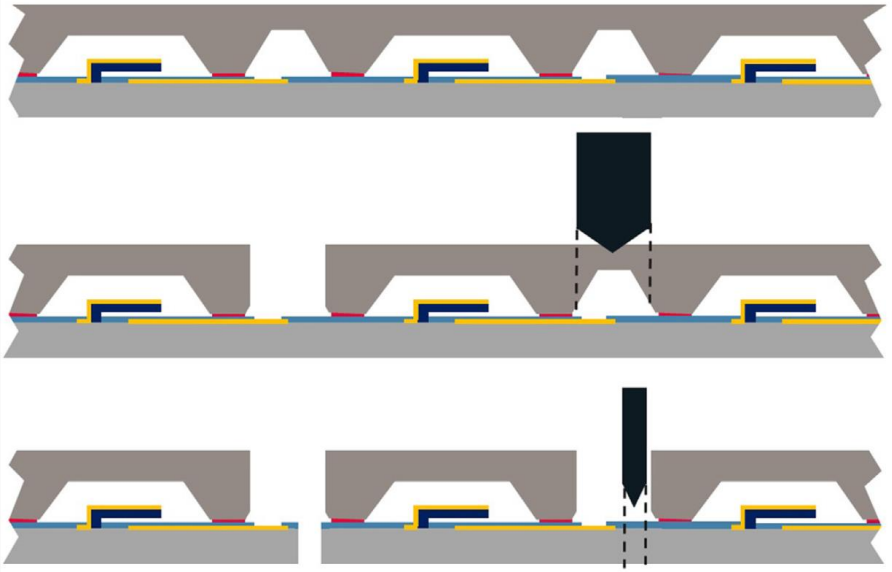


Zero-level packaging: dicing techniques

After wafer bonding, the stack must be singulated but it is also necessary to expose the pads.

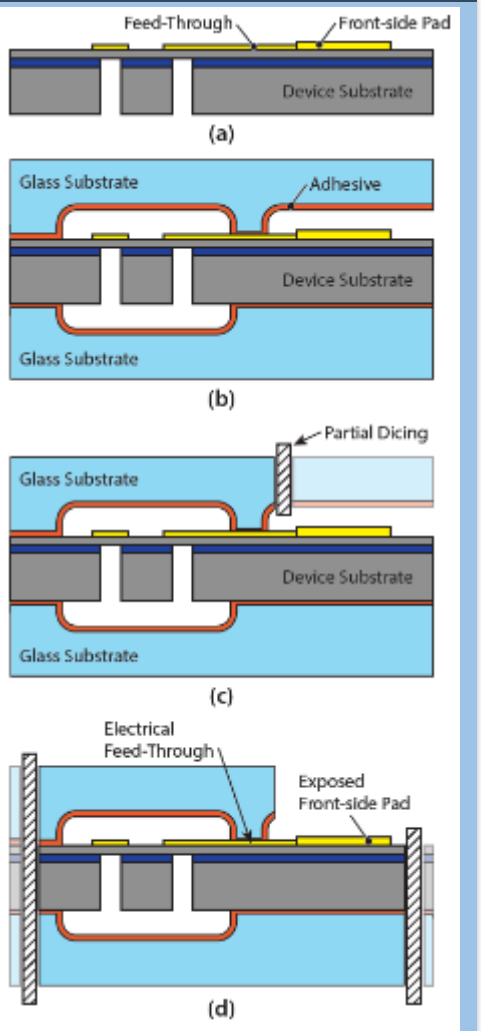
A two-dicing-steps method can be used:

1) Remove the cap wafer material to expose pads
2) Cut through to singulate the dies

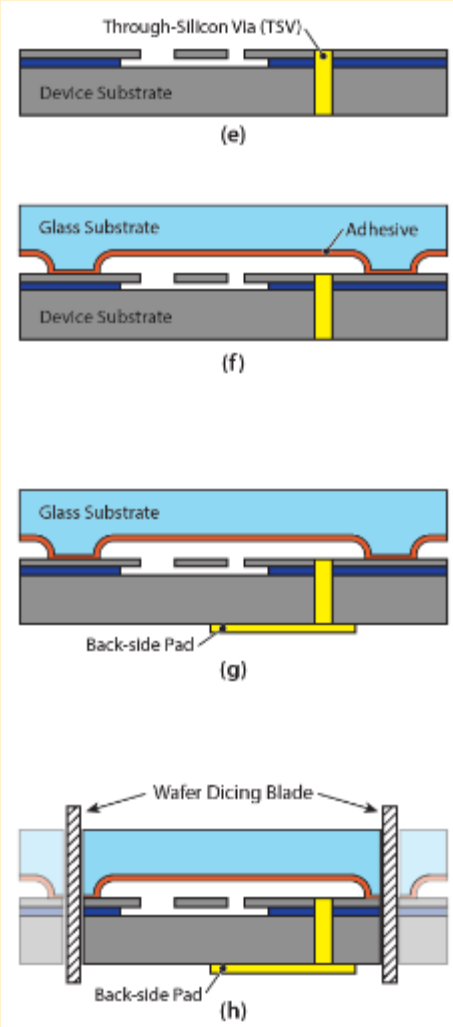


MEMS capping and electrical feed-through

Horizontal feed-through



Through-silicon-vias

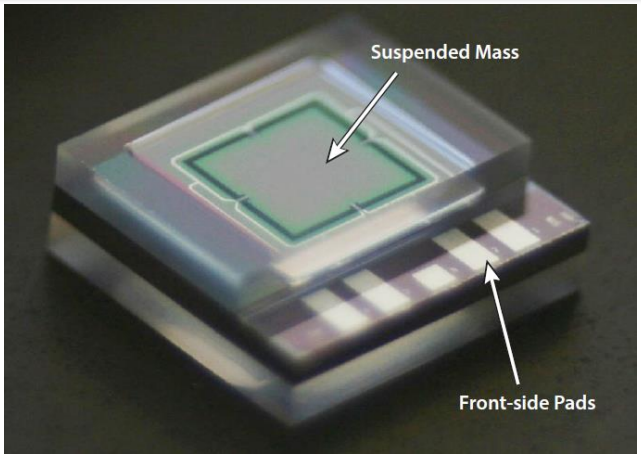


Feedthorugh of electric signals is necessary to enable access to the MEMS pads after capping.

Feed-through can be horizontal, and in this case the two-dicing-steps method is necessary.

Vertical feed-through is more surface efficient, but through-wafer-vias can be a more expensive process.

The best choice depends on several considerations, including **stress compensation** for some MEMS sensors.

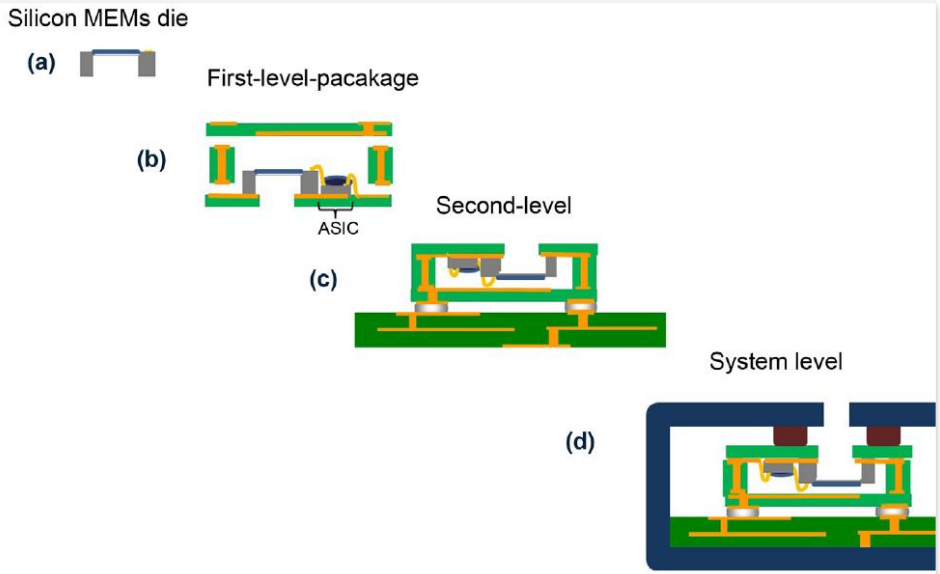


Micromachines **2016**, *7*, 192; doi:10.3390/mi7100192

Examples of pecularities in MEMS packaging

Example 2: MEMS microphone:

- Starting from MEMS die
- **Cavity formation at first-level packaging**
- **First-level packaging: hybrid integration of an ASIC**
- Second-level packaging: *as usual*
- System-level packaging: **sensor exposure**



ASIC integration

MEMS microphones are typically two-chip devices: a MEMS microphone and an ASIC for signal conditioning and amplification.

During first-level packaging, hybrid integration of the two chips can be performed.

Wire bonding is very flexible, but also flip-chip bonding is often used.

Handbook of Silicon Based MEMS Materials and Technologies. DOI: http://dx.doi.org/10.1016/B978-0-323-29965-7.00037-3

Multi-chip hybrid integration: why not wafer-level integration?

Wafer-level integration is very cost-effective, because different chips built with different technologies (MEMS, CMOS) on different wafers could be integrated during wafer processing, before singulation.

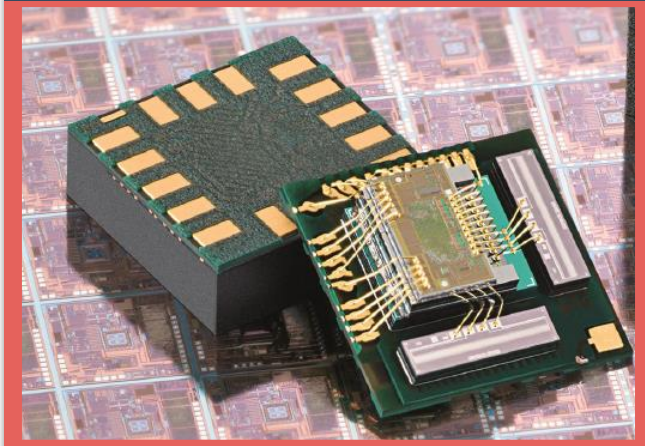
But:

MEMS chips and CMOS chips usually have different characteristics, most importantly size: often few mm^2 are sufficient for CMOS, while larger areas are necessary for the MEMS transducers.

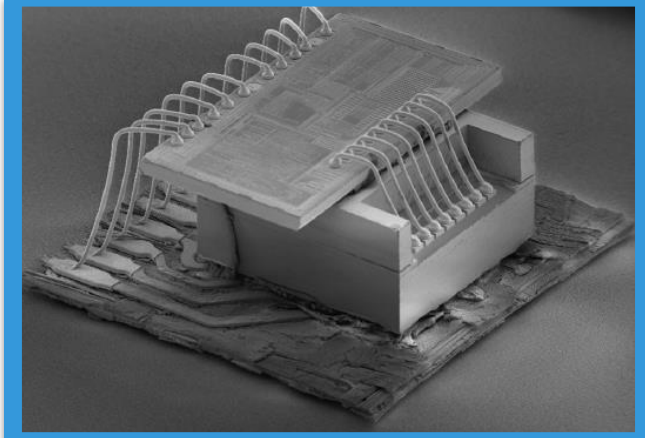
In such case, wafer-level integration would be inefficient, because a relevant part of the CMOS wafer surface would be wasted, just to comply with the MEMS footprint.

Many commercial MEMS sensors are hybrid integrations of MOX and CMOS dies at package level!

Multi-chip assembly: acceleration and magnetic sensor + logic (Bosch Sensortech)



Acceleration sensor (Bosch Sensortech GmbH) with ASIC on top



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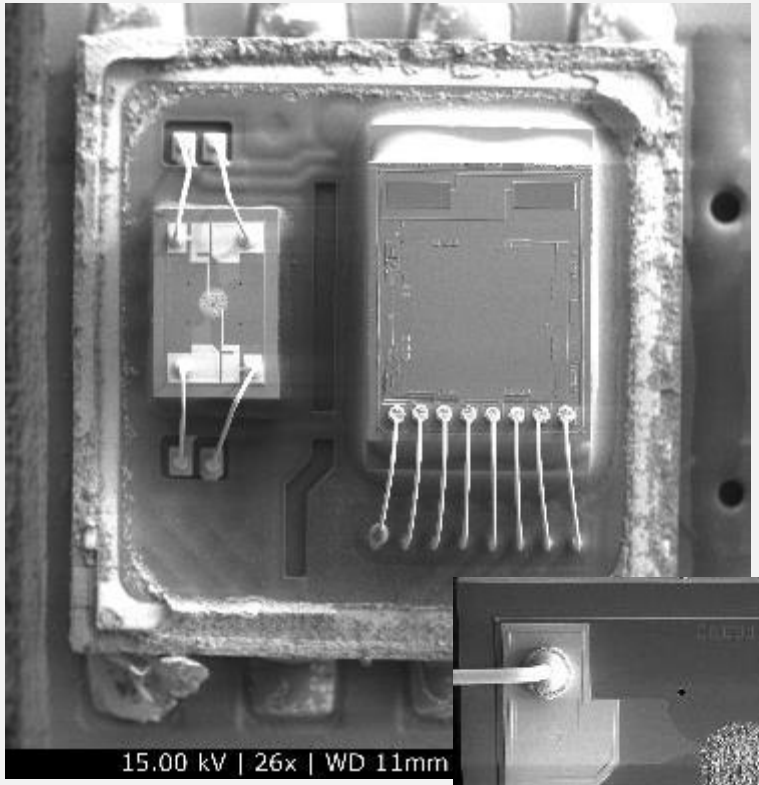
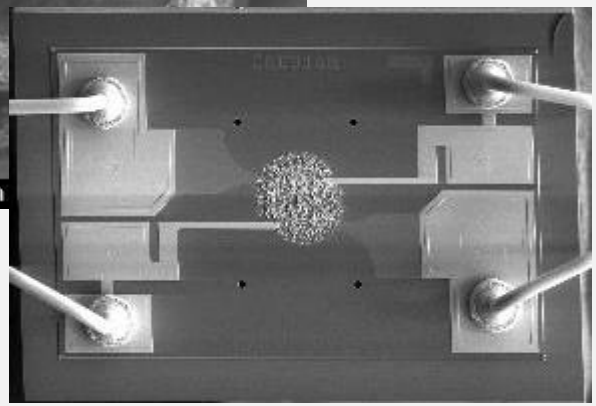
Multi-chip hybrid integration: some more examples

Murata: 2 MEMS dies + ASIC package level int.
(doi: 10.1016/B978-0-323-29965-7.00028-2)

Bosch BME680 sensor system in package

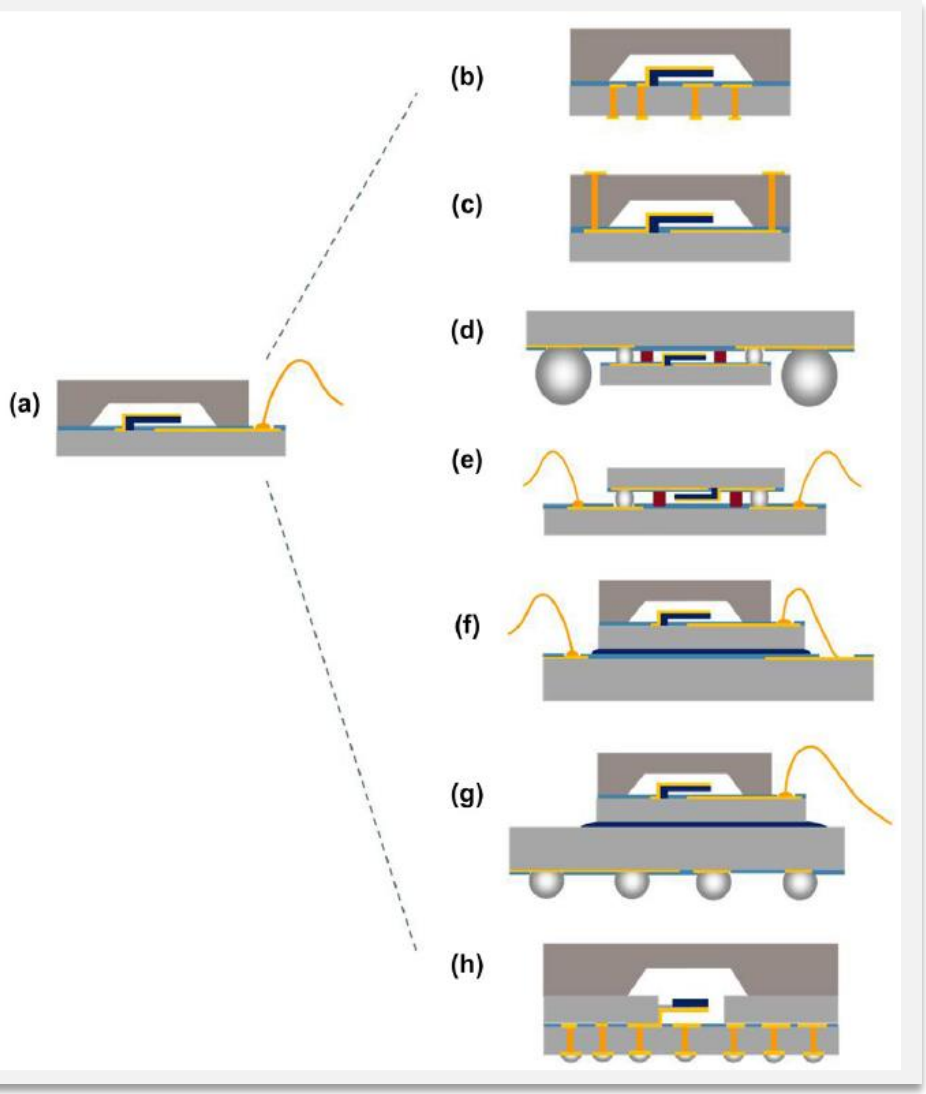
Bosch BME680 gas&pressure sensor: analysis





Source: Twitter
Felix Domke @tmbinc

Steps to 3D integration



Through-silicon vias (TSV)

TSV on cap, with flip-chip

2-level micro-flip-chip

Micro-flip-chip and wire bond

Wire-bond stack

Wire-bond and flip-chip

Silicon interposer with TSV

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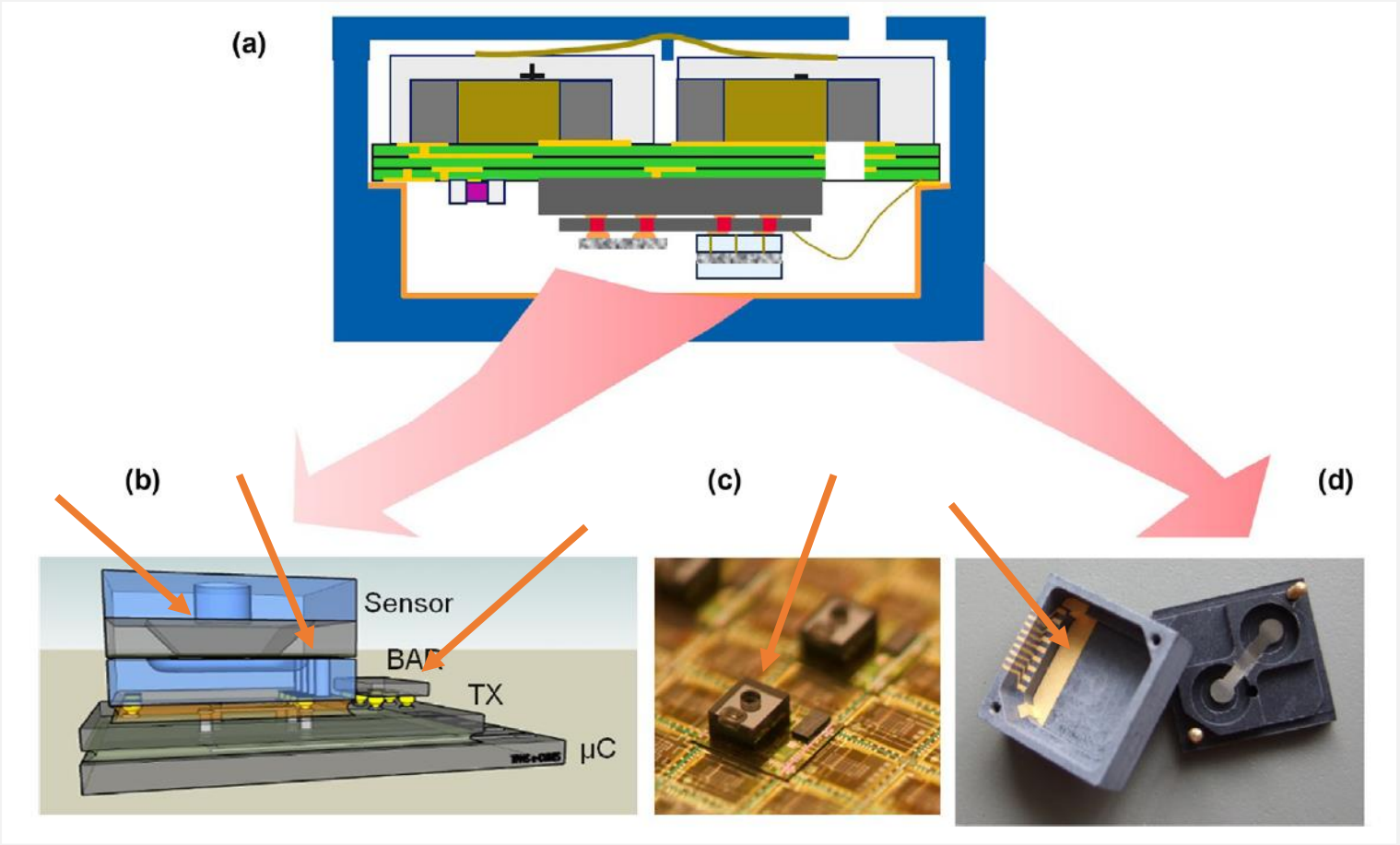
3D integration of MEMS: the vision of «smart dust»



eCUBES demonsrator (european project)

The above figure shows: wafer-level zero-level packaging, through-silicon vias, flip-chip on chip, hybrid integration on microcontroller die, system-level package

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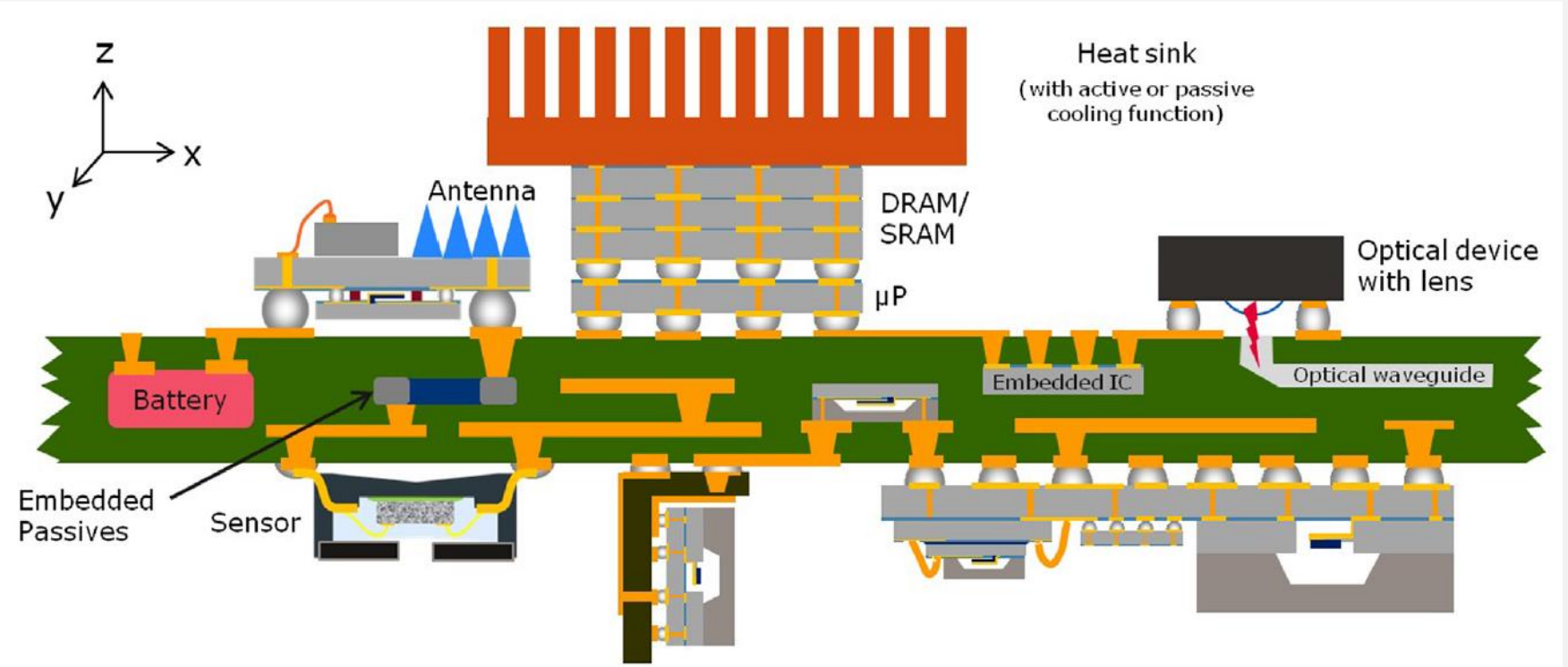
3D integration of MEMS: resuming



eCUBES demonsrator (european project)

Generic sketch of heterogeneous system containing MEMS and several other functions.

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specific cases for microfluidic systems: lab-on-chip and chemical sensing

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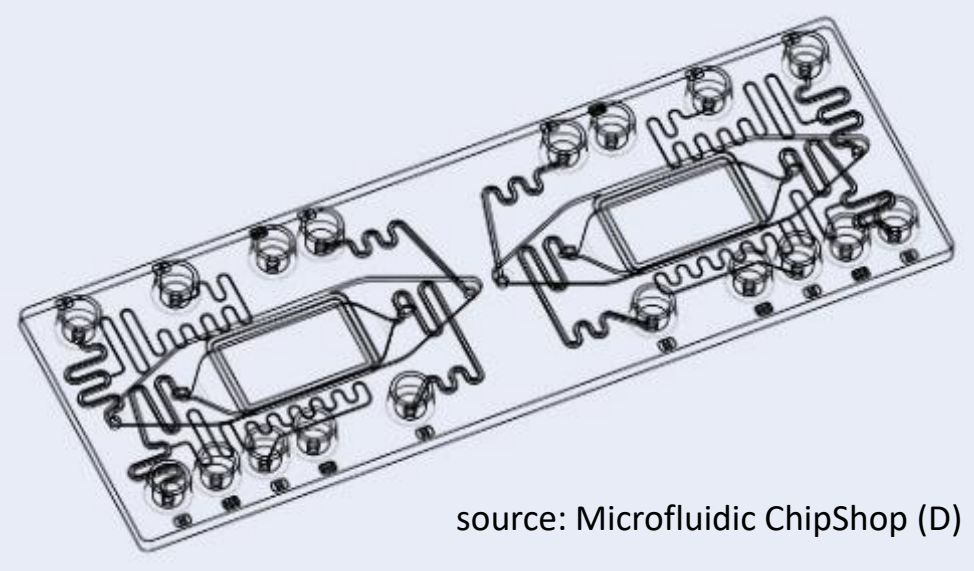
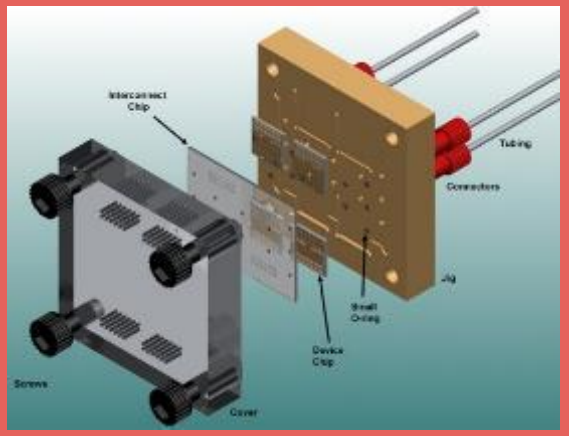
"A lab-on-a-chip (LOC) is a device that integrates one or several laboratory functions on a single integrated circuit of only millimeters to a few square centimeters to achieve automation and high-throughput screening." *(source: Wikipedia)*



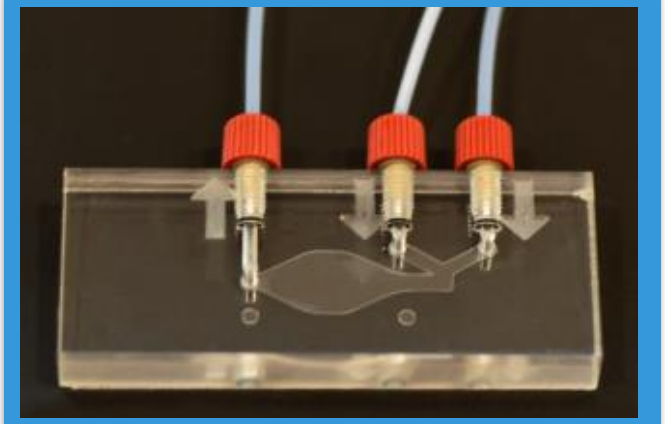
source: Microfluidic ChipShop (D)

Generally, a LOC includes most functionalities required for analysis, but not all of them. Most LOCs must be connected to external hardware for pumping and detection.

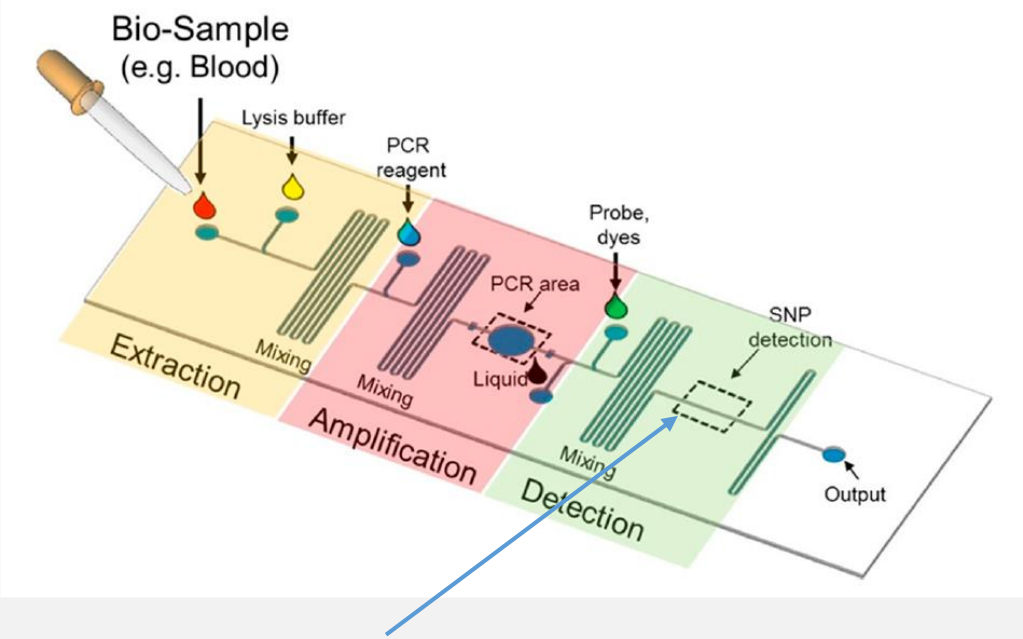
S.Miserendino et al, Caltech
doi:10.1016/j.sna.2007.07.019



Cherry Biotech Therma Chips



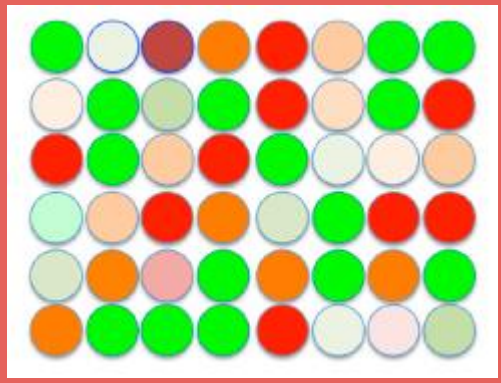
Lab-on-chip: typical functionalities on chip and analysis sequence



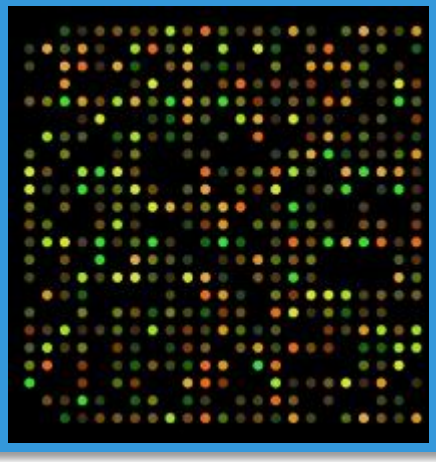
Fluorescence detection of labelled markers is usually performed off-chip!

source: Chao-Wei Huang et al.
doi: 10.3390/microarrays4040570

Differently labelled targets are immobilized in the detection region



Typical microarray fluorescent image
Source: Western Oregon University

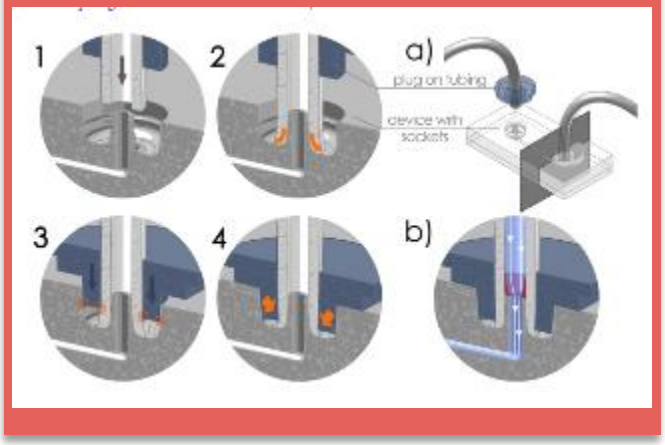


source: Oregon University Online Chemistry Textbook
CH 450 and 451: Biochemistry

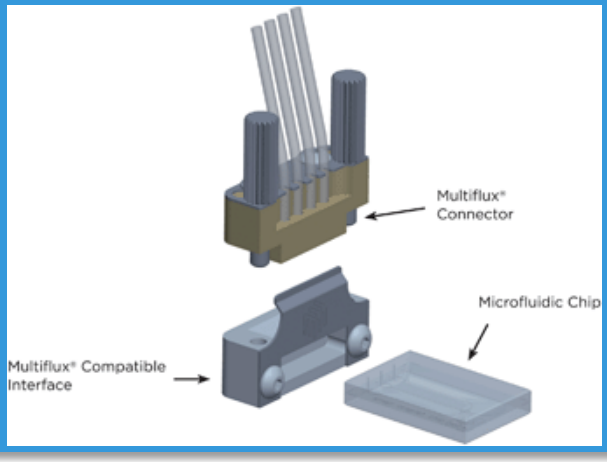
Usually, the LOC is only the disposable part of the entire sensing system. This makes perfect sense, since the disposable part benefits from low-cost and miniaturization, while these features are not mandatory for the entire system.

source: Microfluidic ChipShop (D)

Andrea Pfreundt et al, doi:10.1088/0960-1317/25/11/115010



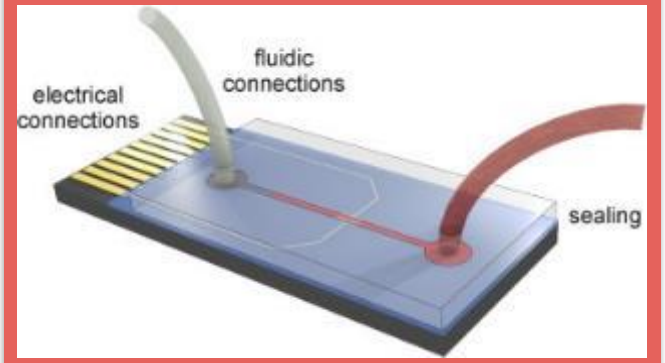
H. Van Heeren, doi: 10.1039/C2LC20937C

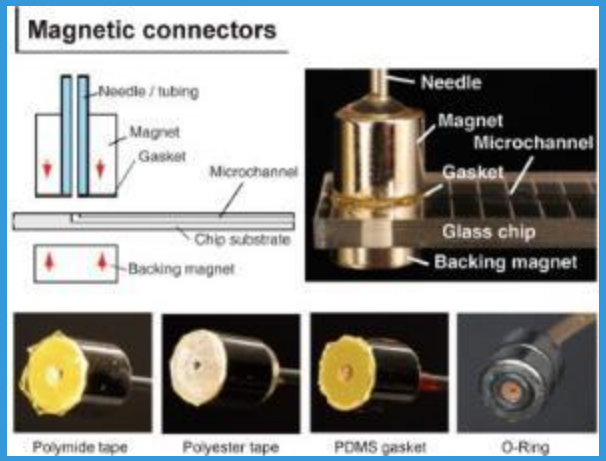


Typical requirements for LOC interconnects:

- Reversibility
- Low dead volume
- Chemical inertness
- Biocompatibility
- Temperature resistance
- Easy alignment / self-alignment
- Low leak
- Low cost
- Long shelf-life
- …

Y. Temitz et al,
doi:10.1016/j.mee.2014.10.013

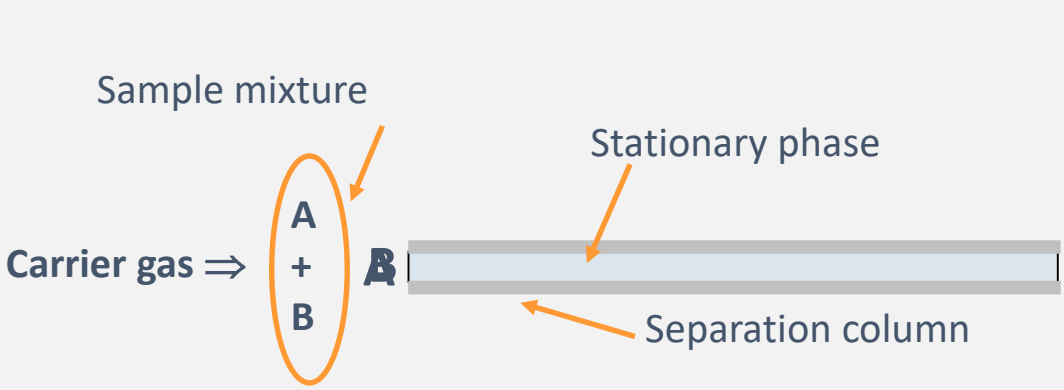


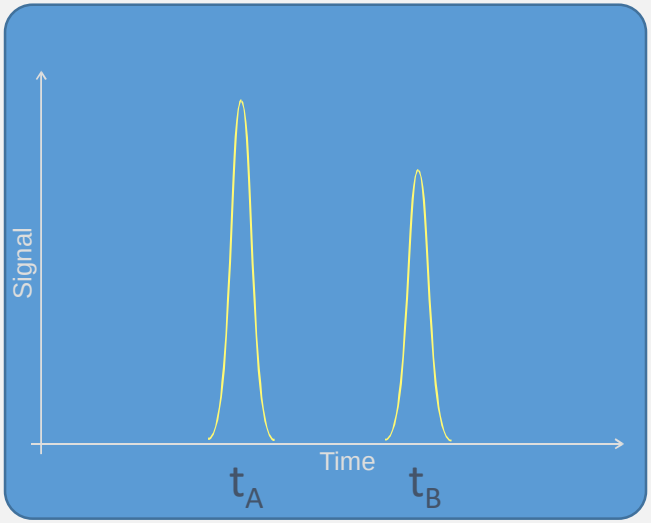


Gas-chromatography (GC)

Gas-chromatography is a well established technique for the chemical analysis of complex real-world samples.

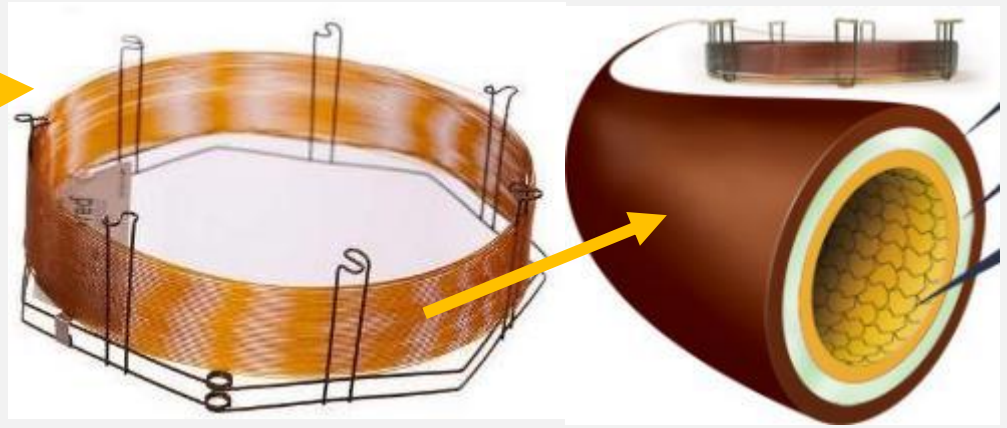
The gas-chromatographic separation principle:
Based on specific affinity between sample and "stationary phase"





μTAS and lab-on-chip examples

Typical GC system



MEMS-based GC system

Photographs courtesy of ION-GAS GmbH, Dortmund (Germany)

A complete gas-chromatograph on a Silicon wafer

In 1979, a very visionary publication proposed a complete GC system on a 2'' silicon wafer.

Yet, this strategy was never exploited. The yield would be only 1 device per wafer!

A Gas Chromatographic Air Analyzer Fabricated on a Silicon Wafer

STEPHEN C. TERRY, MEMBER, IEEE, JOHN H. JERMAN, AND JAMES B. ANGELL, FELLOW, IEEE

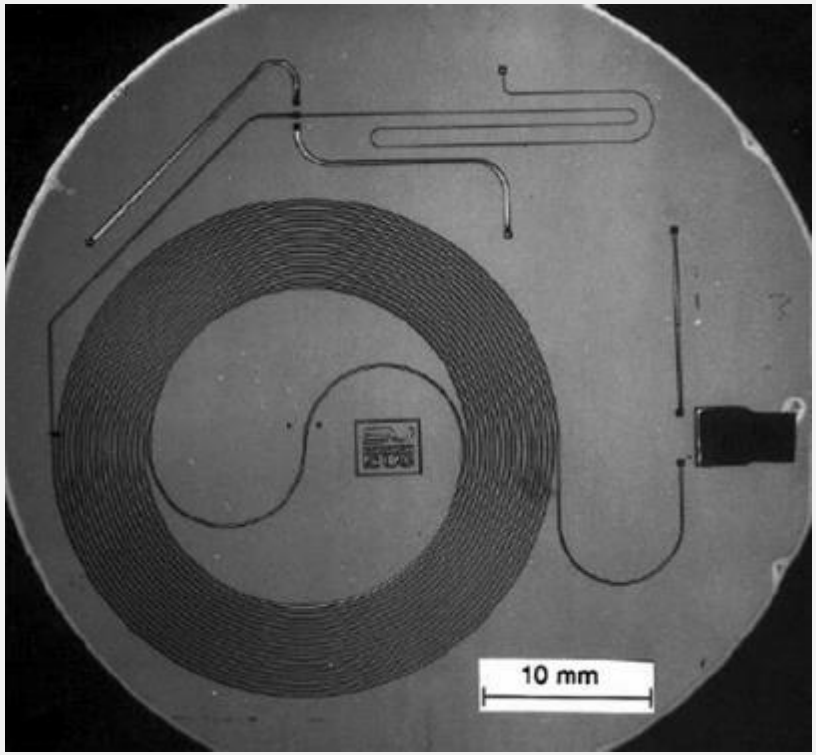
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-26, NO. 12, DECEMBER 1979

The inefficient use of the wafer surface is evident.

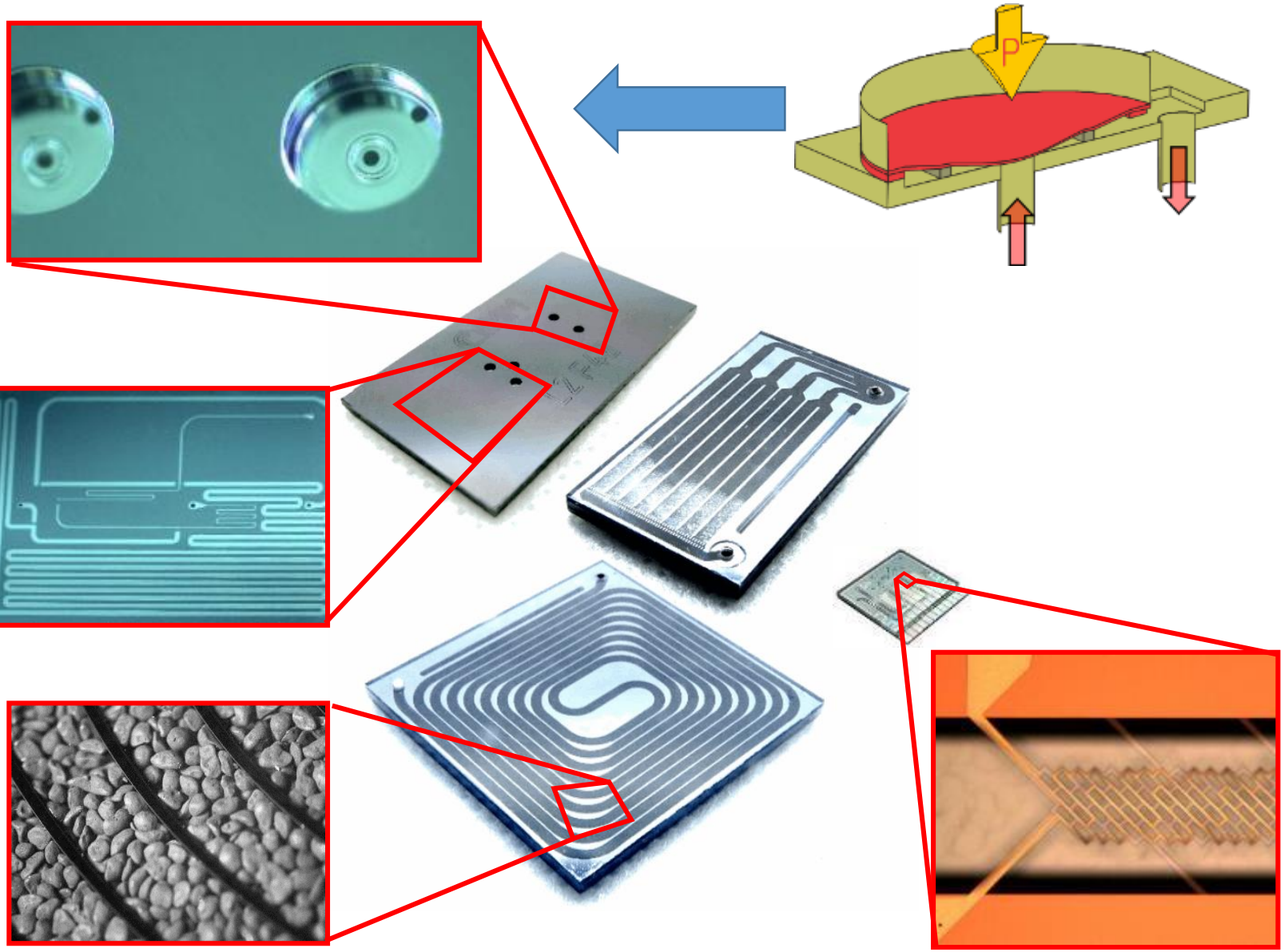
Furthermore, usually different parts of the GC must be at different temperatures:

- GC column runs a temperature ramp
- Detector must stay in isothermal conditions

➔ "3D integration" could be useful!

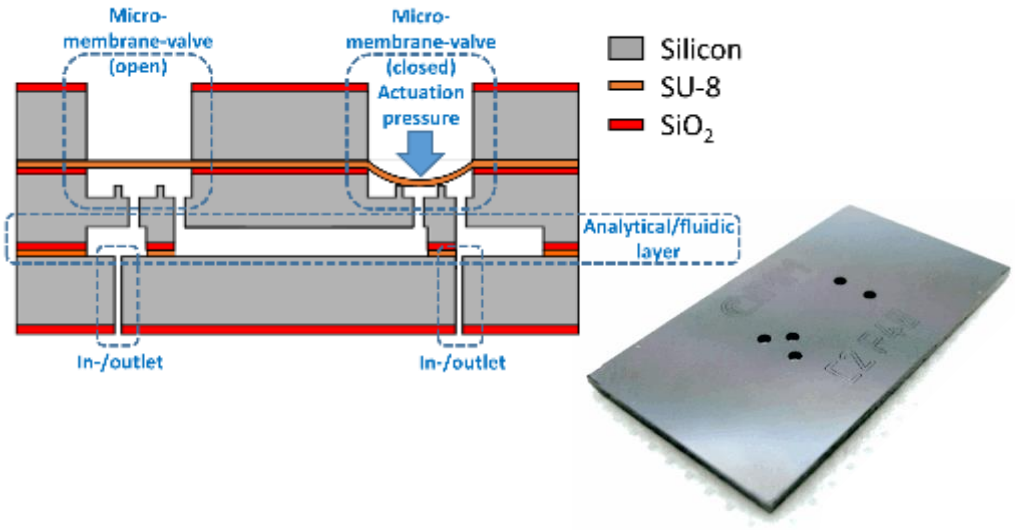


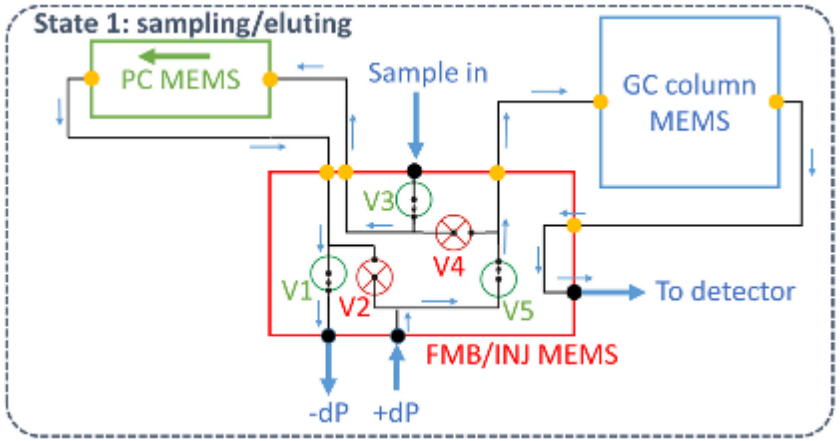
Example: MEMS components of a micro-GC system



Example: MEMS components of a micro-GC system

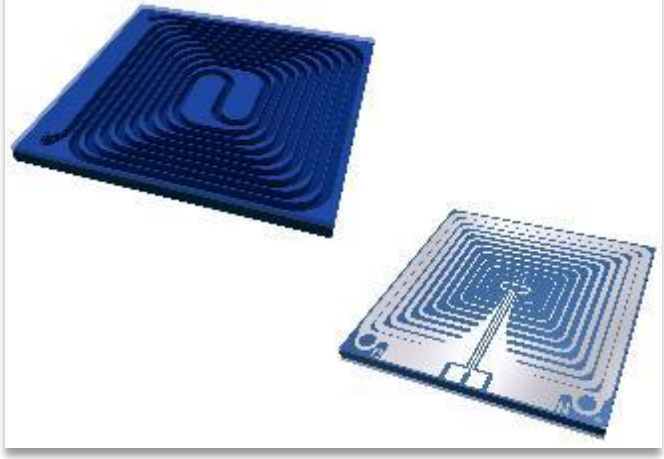
MEMS injector





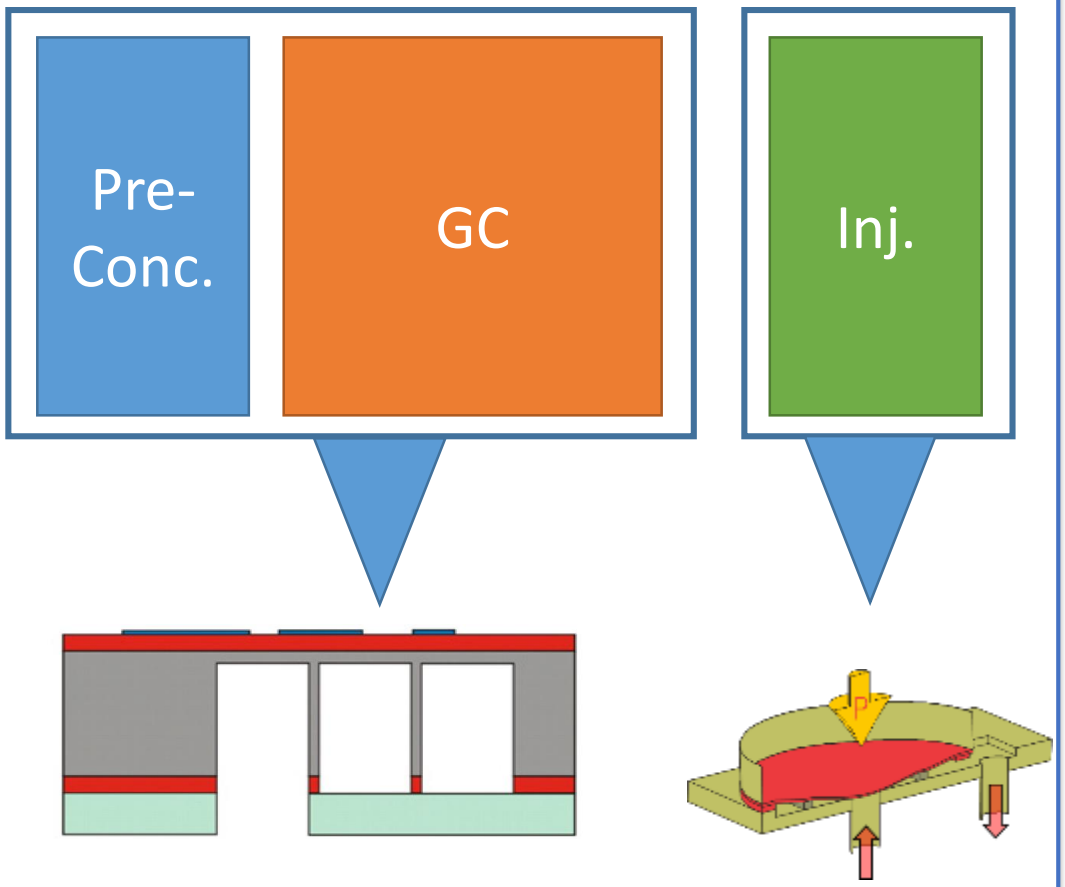
MEMS pre-concentrator

MEMS GC column

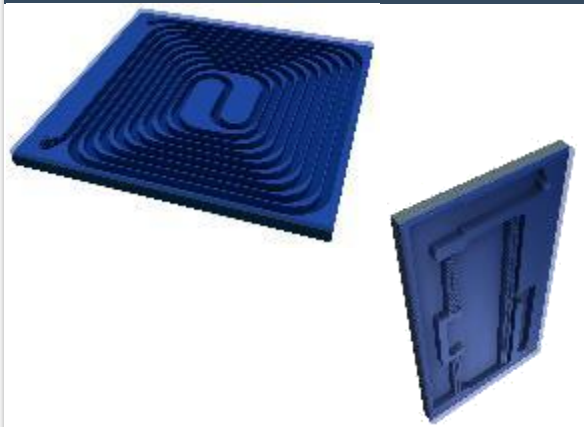


Example: MEMS components of a micro-GC system

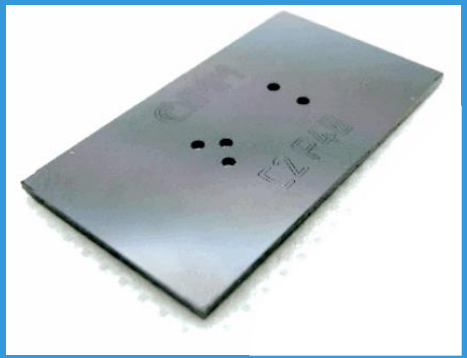
MEMS sizes and technology



GC and Pre-Concentrator



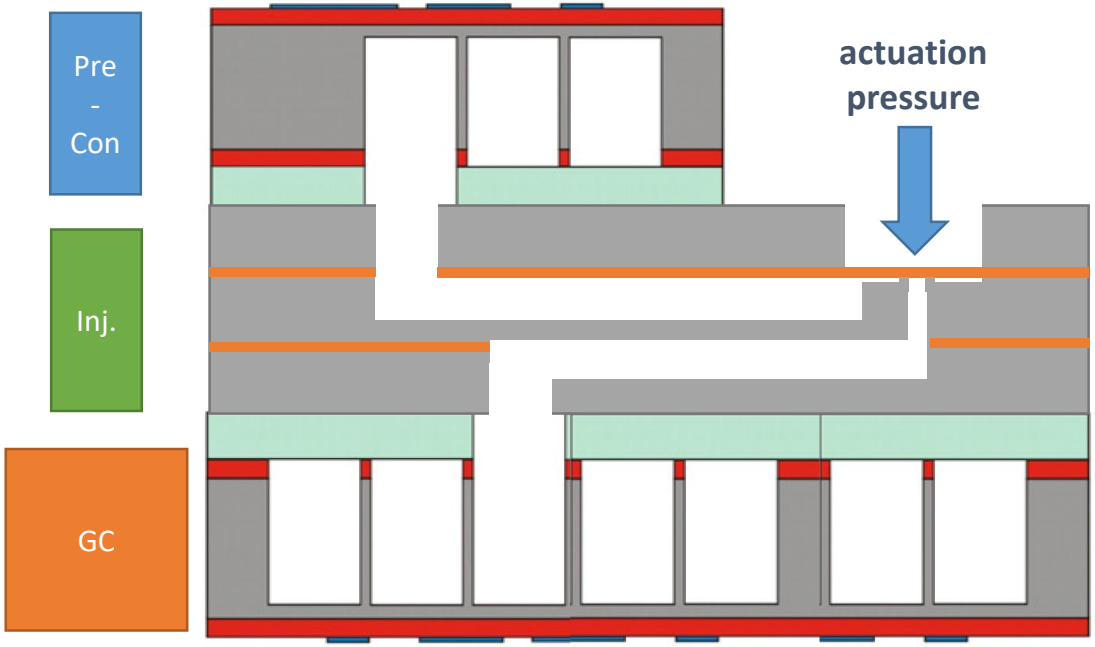
Injector



Proposal: wafer-level integration of a complete micro-GC

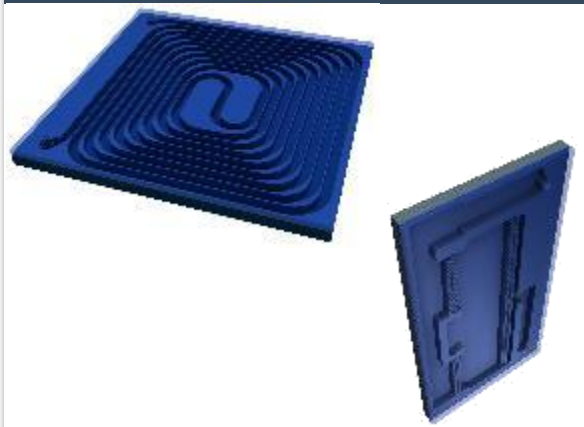
Design study for a wafer-level integrated micro-GC

7-wafer stack!

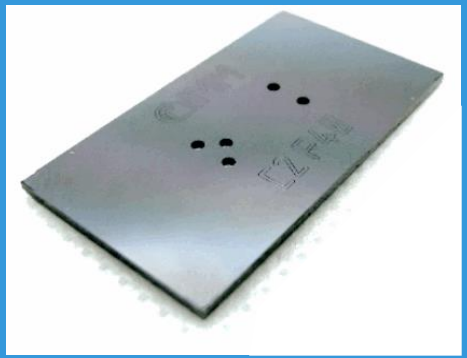


- **A lot of pre-concentrator wafer area is wasted**
- **Injector area is larger than needed**
- **And: temperature…**

GC and Pre-Concentrator

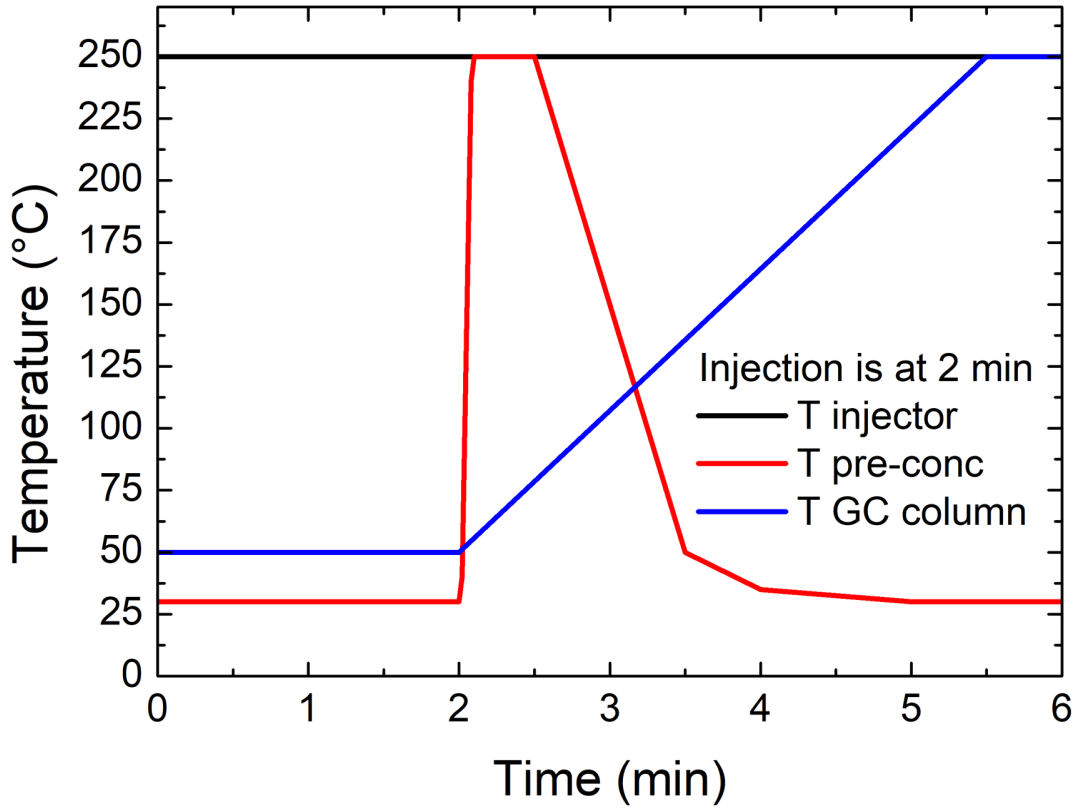


Injector

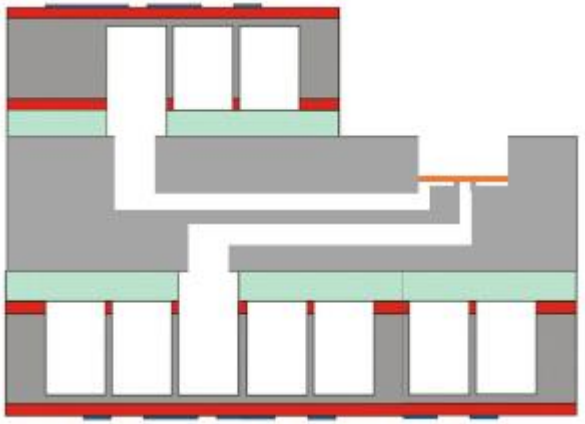


Another drawback, specific for micro-GC analysis system

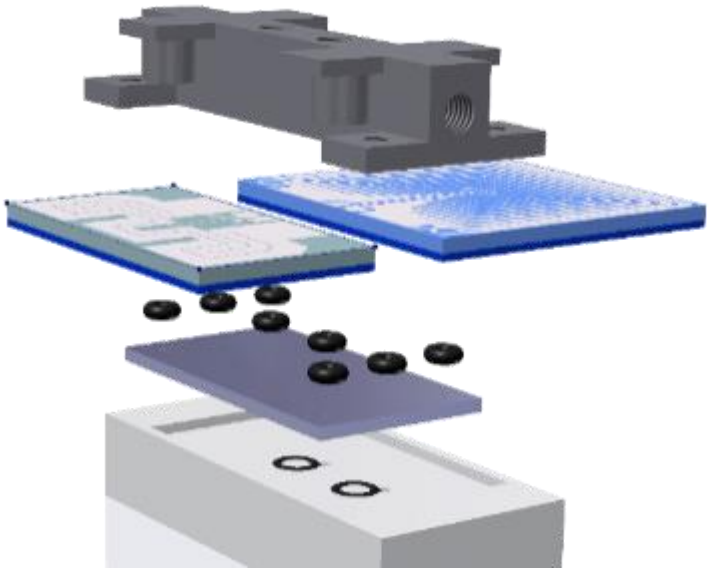
Typical temperature profile of the three GC components during an analysis cycle:



Is it possible to apply such a temperature cycle to this chip?

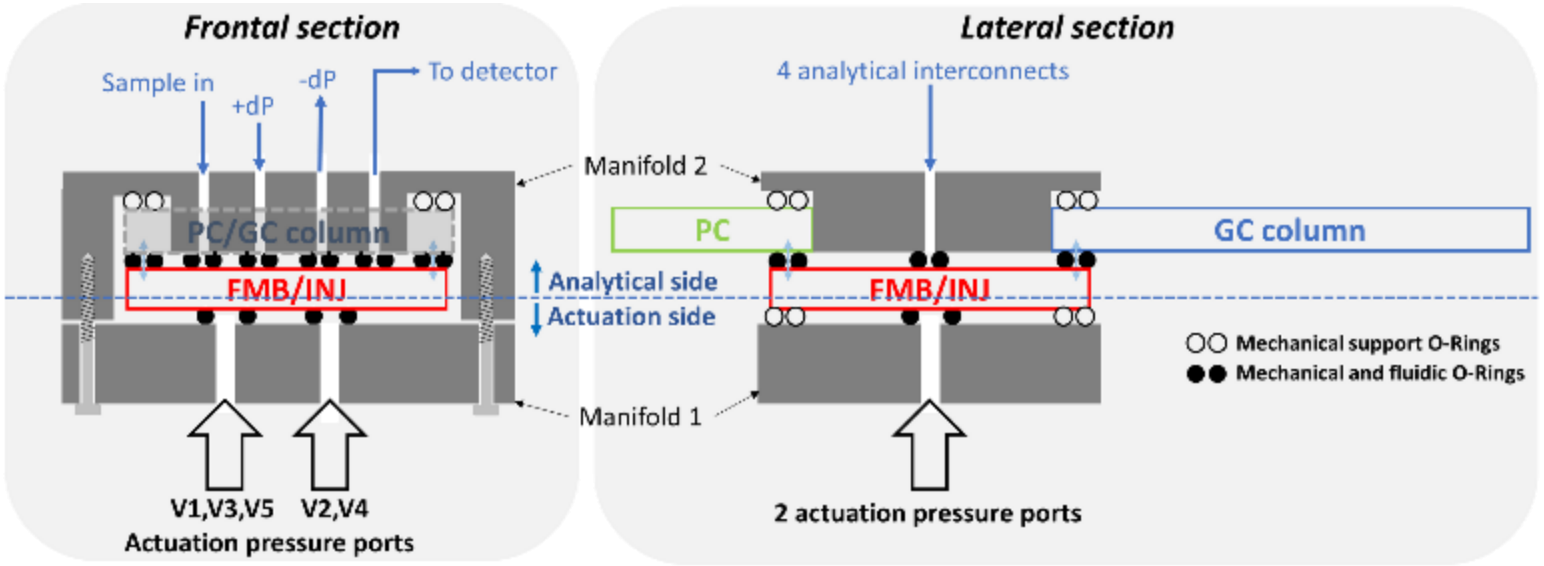


A possible solution for analysis systems: system-level integration

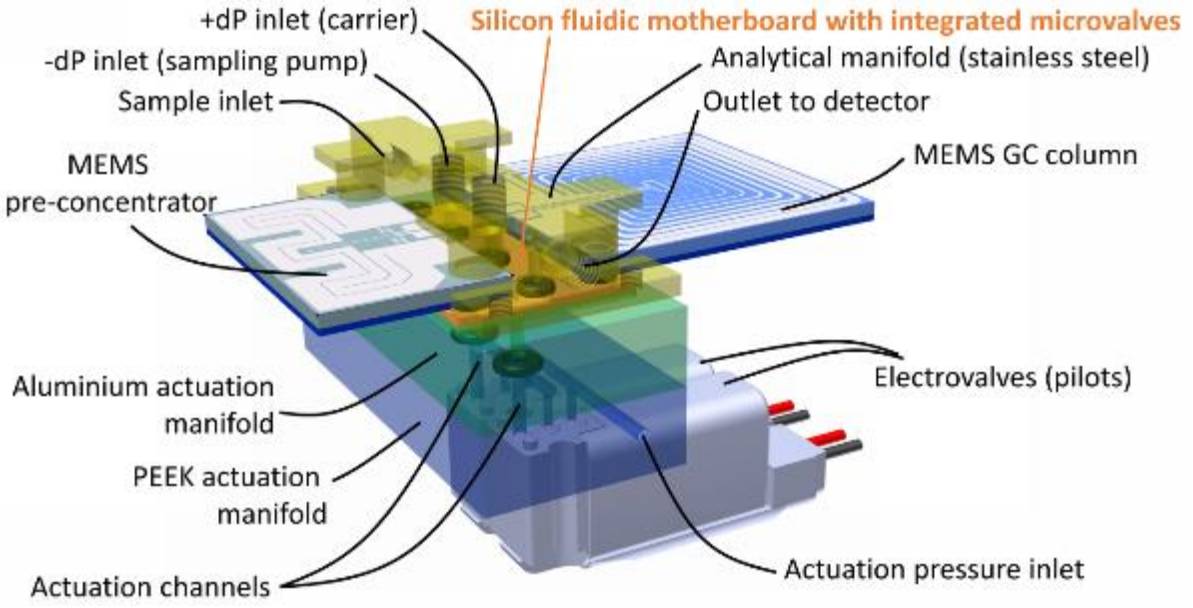


Benefits

- **Optimized use of wafer surfaces**
- Flexible
- Reversible
- Easy to replace single parts
- Temperature independence of the single MEMS devices
- O-Rings are inert and temperature resistant

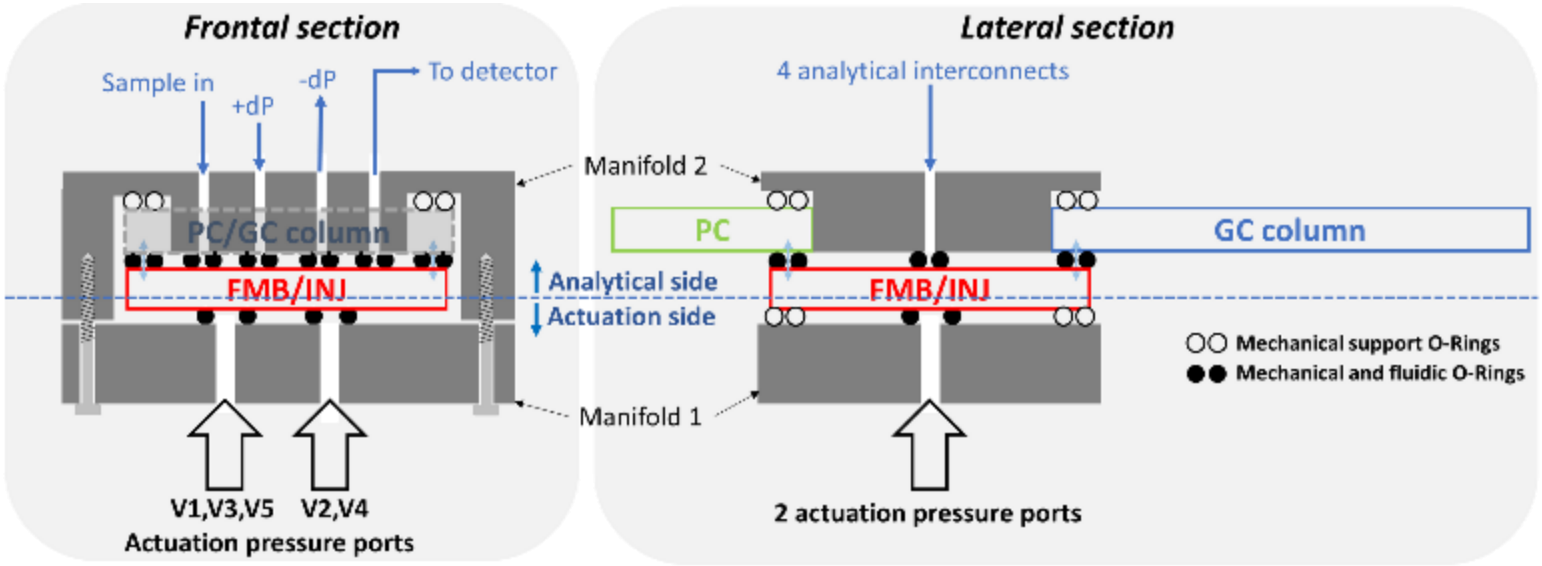


A possible solution for analysis systems: system-level integration

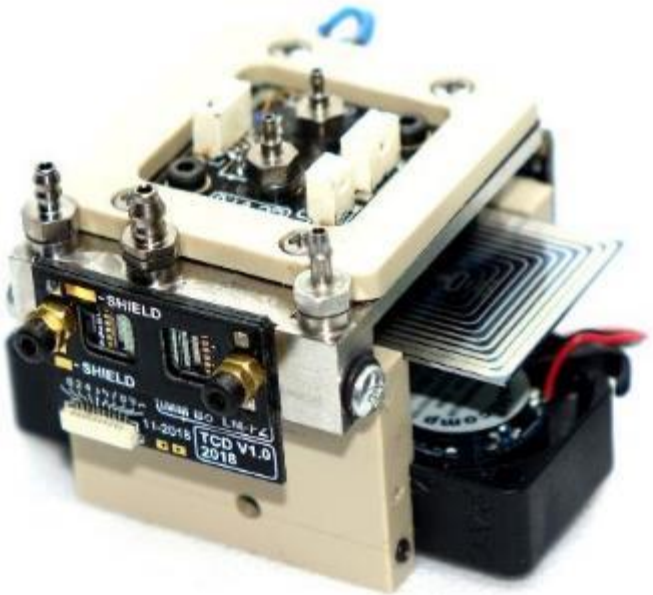


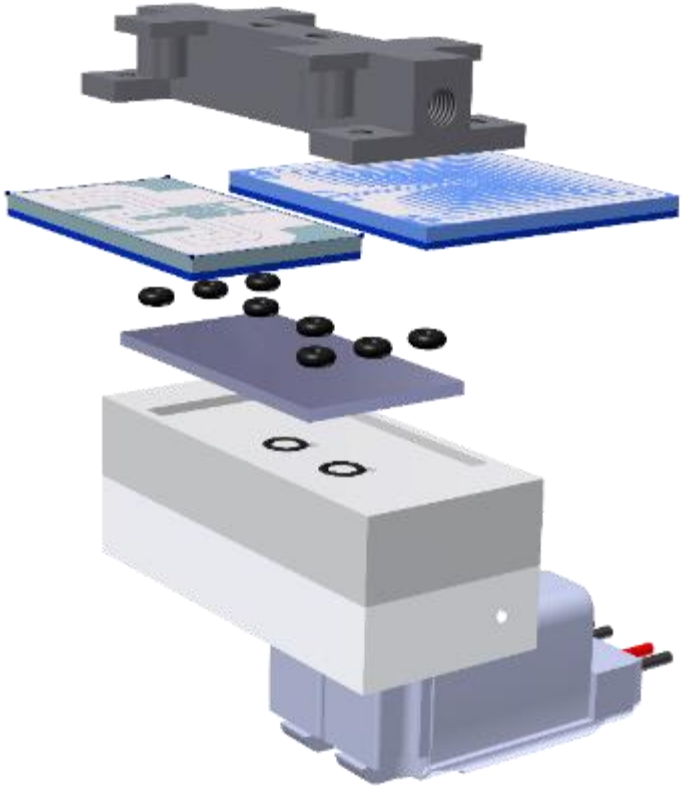
Drawbacks

- Not a wafer-level process
- Slightly higher dead volumes
- Complexity transferred from MEMS level to assembly level



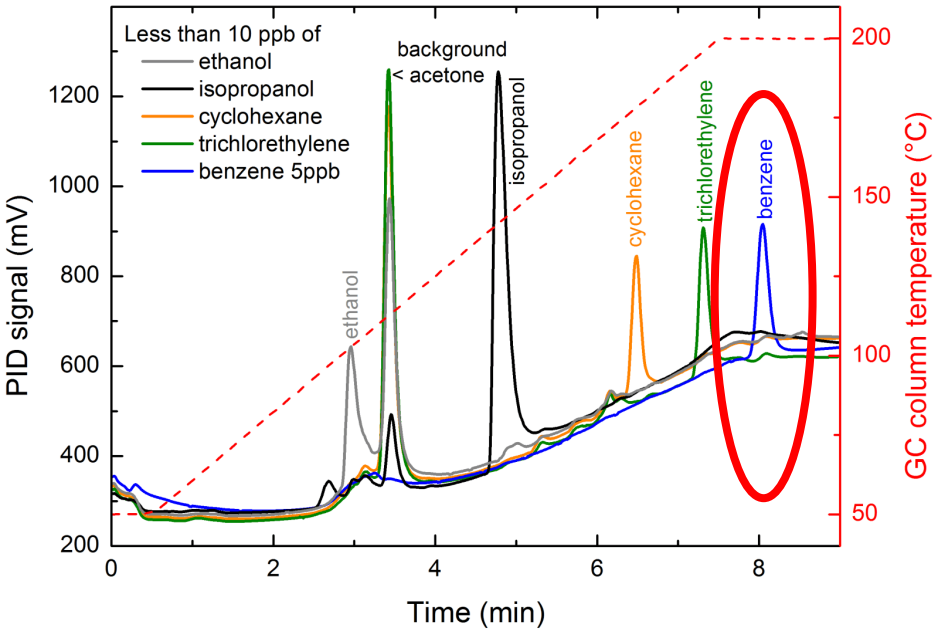
compact-GC platform: TD/GC/TCD



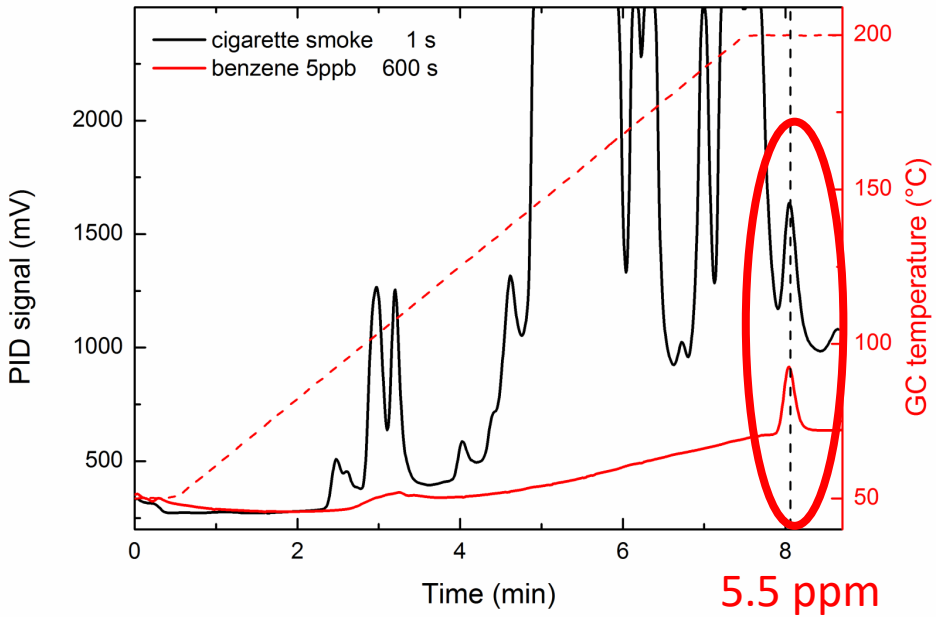


The compact-GC platform: sensing examples

Monitoring of indoor pollutants

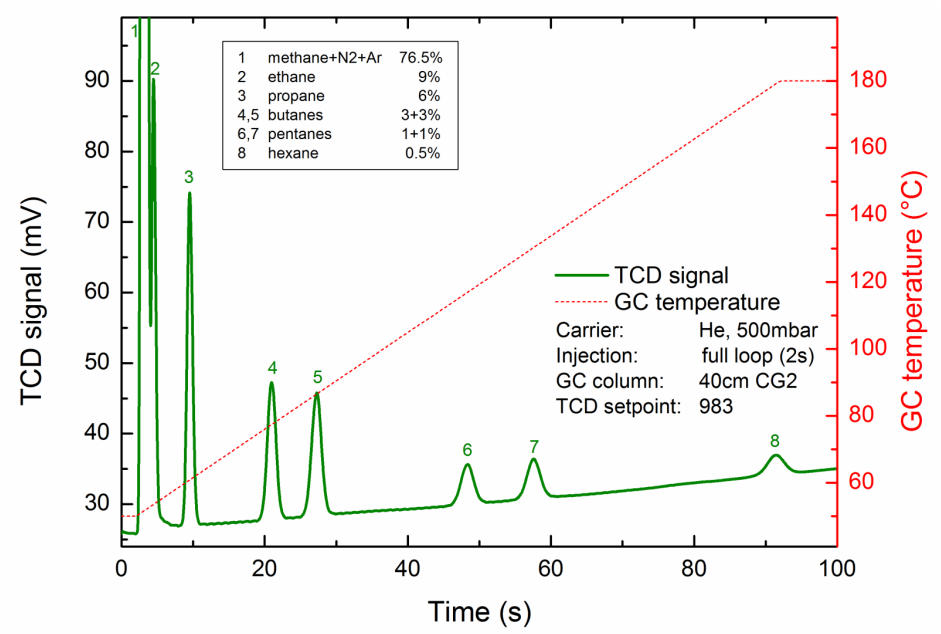


Benzene in cigarette smoke

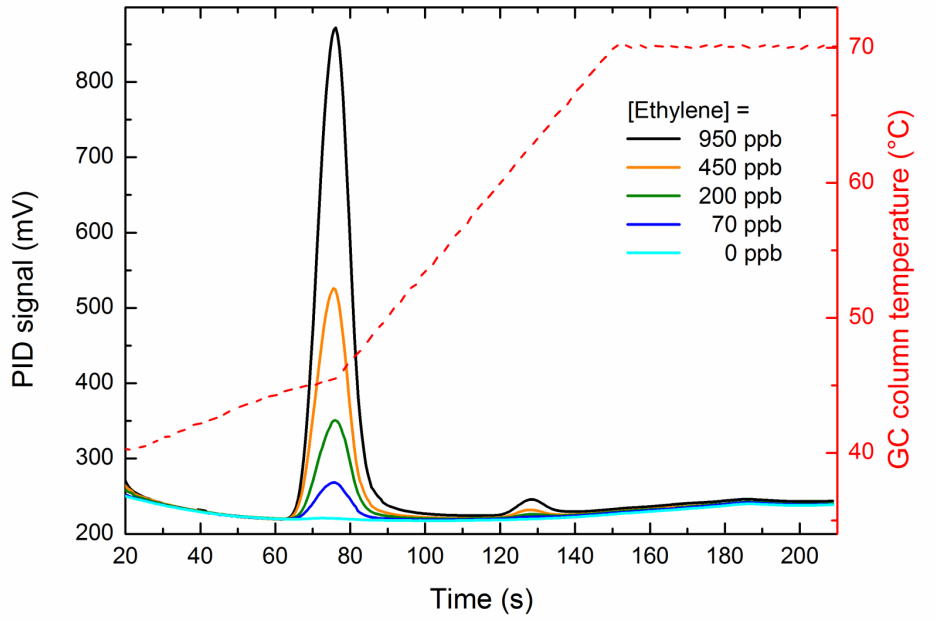


The compact-GC platform: sensing examples

Natural gas composition: **determination of calorific power**



Ethylene: monitoring of fruit ripening stages



Resuming:

- **MEMS packaging often has special requirements, making usual electronic device packaging technologies unsuitable:**
  - **Zero-level packaging, e.g. for cavity formation**

- **In most cases, the ASIC is not on the same wafer as the MEMS:**
  - **System-in-package combining several dies and different technologies**
    - **Allows for optimized use of Silicon area**
    - **Generally cost-effective in most cases**
    - **Allowing for in-package 3D integration**

- **Some MEMS devices have additional requirements, e.g.:**
  - **Lab-on-chip: need for external parts → reversible fluidic connections**
  - **Chemical sensors: different temperature profiles on different dies**
  - **Viable routes:**
    - **Easily disposable and rapidly replaceable chips (LOC)**
    - **System-level 3D integration (micro-GCs)**

Thank you for your attention