PHOTONICS PACKAGING
Laser hybrid integration towards space applications

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OUTLINE

1. *INTRODUCTION TO PHOTONICS PACKAGING.*
   - *1.1. Definition*
   - *1.2. Main Processes*
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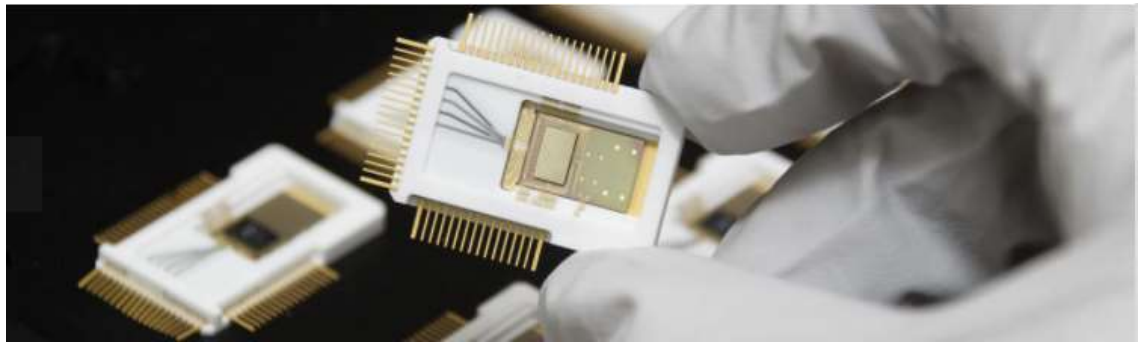
   - *2.2. Hybrid vs Monolithic Integration*
   - *2.3. Flip Chip Bonding*
   - *2.4. A Real Case – SOA Integration*
3. *PHOTONICS PACKAGING FOR SPACE APLICATIONS*
4. *CONCLUSION*



1. Introduction to Photonics Packaging

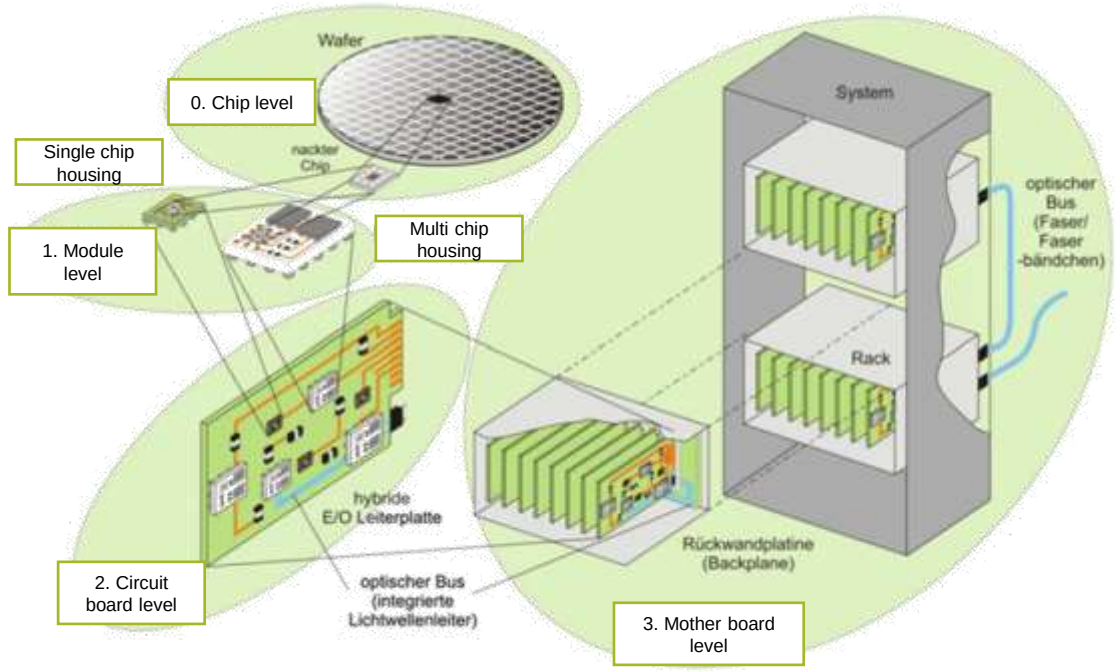
1 INTRODUCTION TO PHOTONICS PACKAGING
1.1. DEFINITION

INTEGRATED PHOTONICS

Emerging technology for optical telecommunications and optical interconnects in microelectronics
Established CMOS fabrication technologies used in silicon electronics

How can we interface the PIC with the outside world?
How can we pass from bare chip to a working component?

PACKAGING



PACKAGING LEVELS IN A COMMUNICATION SYSTEM
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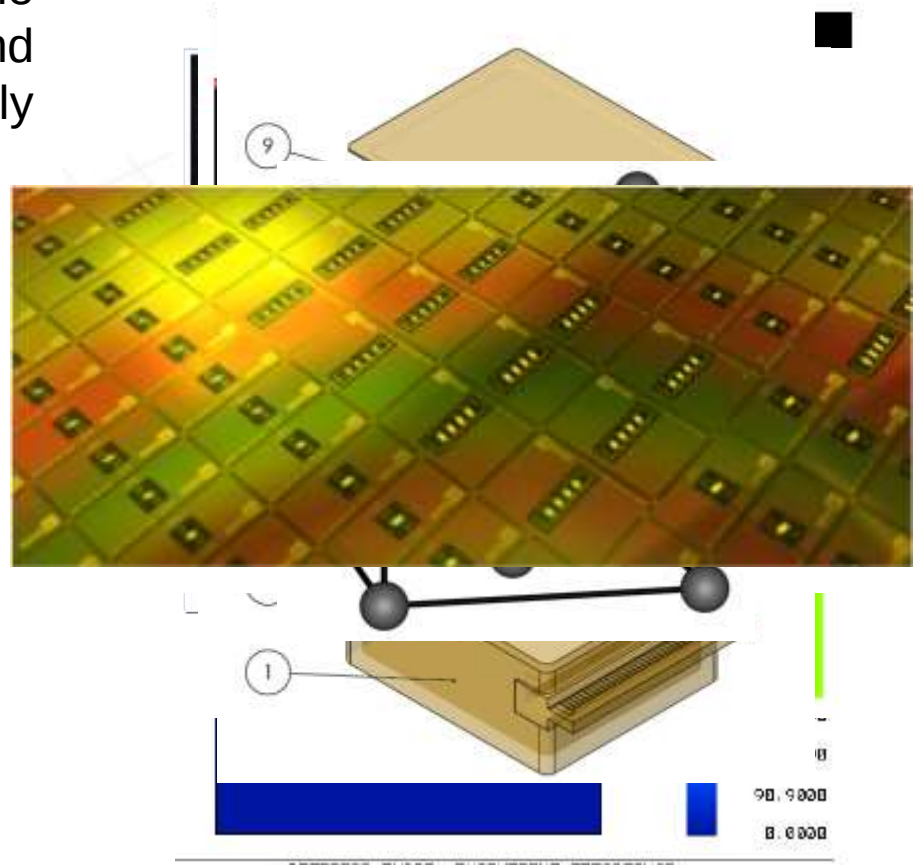
1 INTRODUCTION TO PHOTONICS PACKAGING
1.1. DEFINITION

Definition

- Techniques and competences needed to realize the optical & electrical connections between the PIC and the outside world, in a stable and environmentally adapted housing.
- Everything between chip and the system.

Includes

- High-frequency technology
- Classical optics/wave optics.
- Fiber alignment.
- Precision engineering design and CAD design
- Cooling/heat management
- Communications engineering
- Solid-state physics
- Etching of silicon substrates
- Thick/thin-film technology
- Gluing, soldering, welding, bonding technology



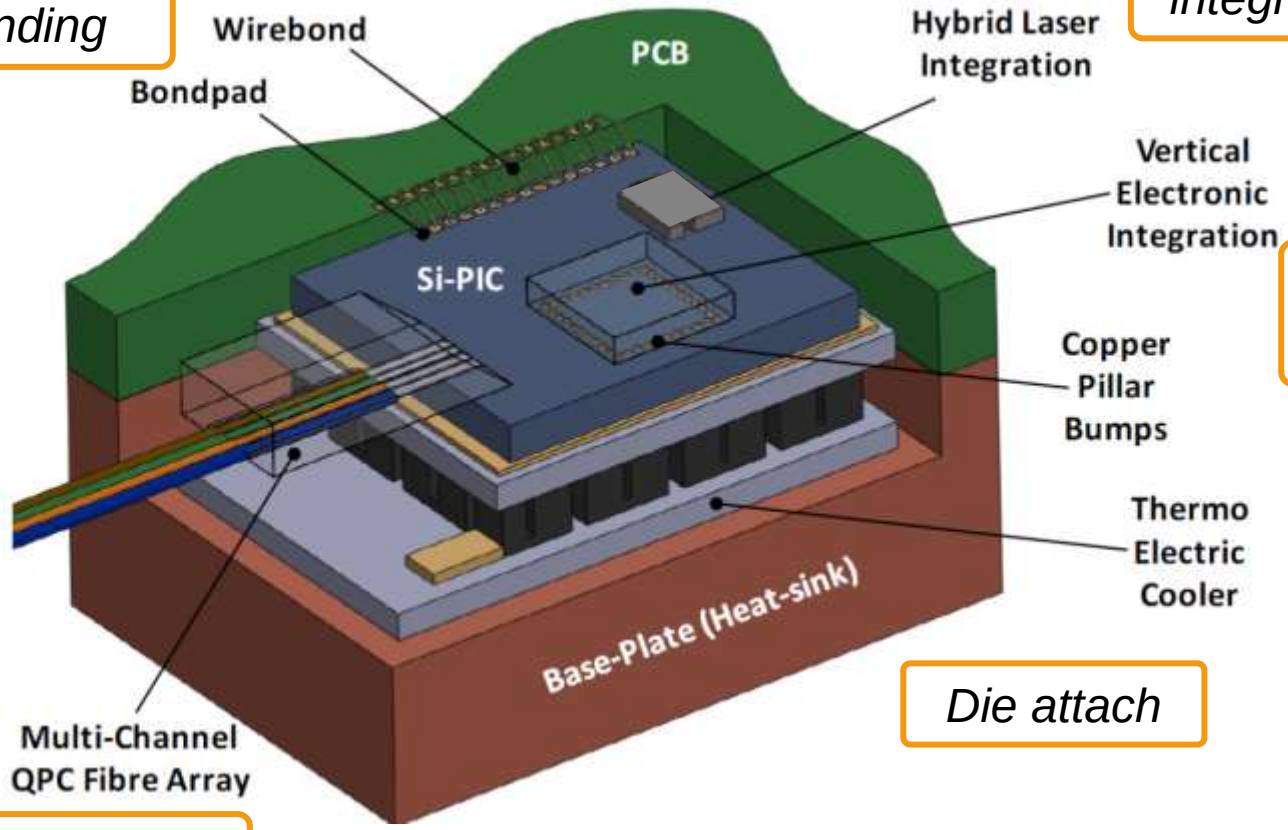
1 INTRODUCTION TO PHOTONICS PACKAGING
1.1. DEFINITION

Elements Covered By Photonics Packaging Of Si - PIC

Wire bonding

Housing

Laser integration



Flip chip bonding

Die attach

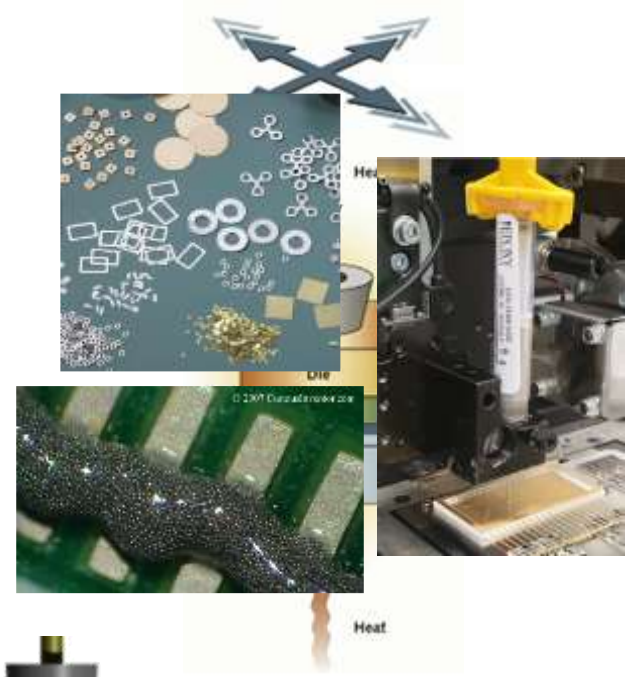
Fiber PIC coupling

Appl. Sci. 2016, 6, 426; doi:10.3390/app6120426 (modified)

1 INTRODUCTION TO PHOTONICS PACKAGING
1.2. PROCESSES

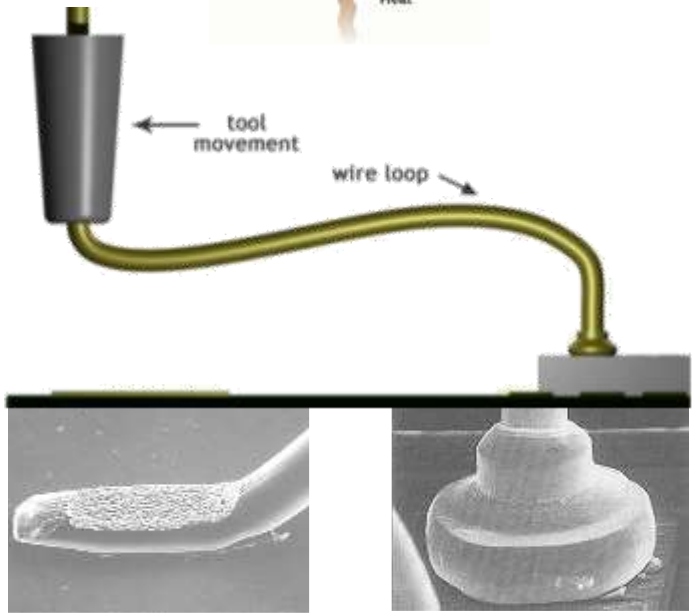
Die attach

- Refers to attach a die to a substrate, base package, a board or any combination of them.
- Solder preforms, solder paste, metal-filled epoxies.
- Mechanical stability, heat conduction.
- Die+ pick up tool, substrate+ heating plate.



Wire bonding

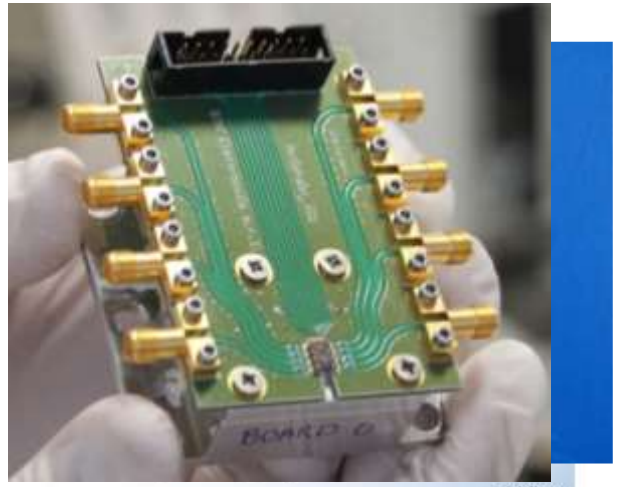
- Electrical interconnection technique.
- Welding Au or Al wires between the chip pads & package contacts.
- Capillary, heat, pressure and/or ultrasonic energy.
- Ball bond, wedge bond.



1 INTRODUCTION TO PHOTONICS PACKAGING
1.2. PROCESSES

Housing

- PCB
- Common type of packages in optoelectronics: dual in line, butterfly...
- Optical output:
  - Plated ferrule, fiber output.
  - Receptacle, pluggable output.



Hermetic sealing

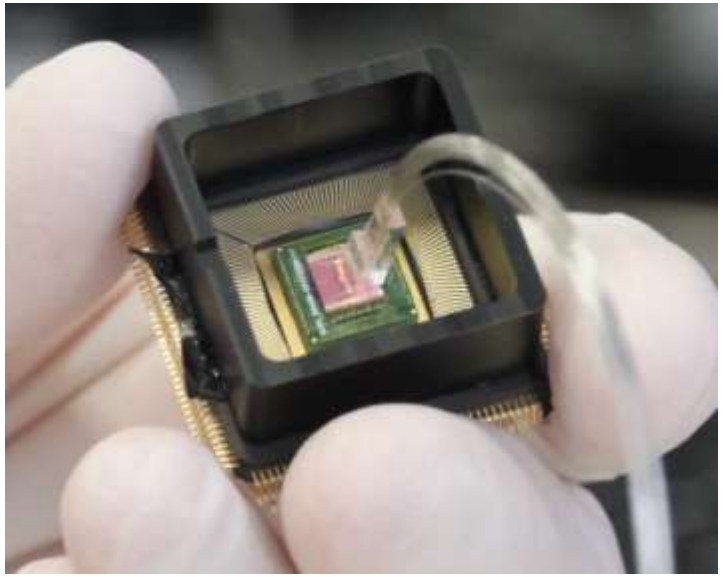
- Prevent intrusion of contaminants (moisture) into a package.
- Hermetic package must be metal or ceramic, polymers are permeable.
- Methods: welding or soldering.

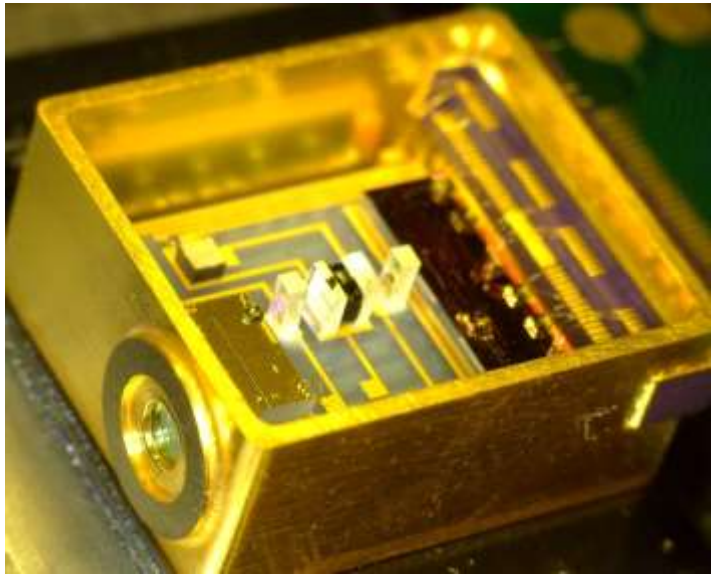
PARALLEL SEAM WELDING:

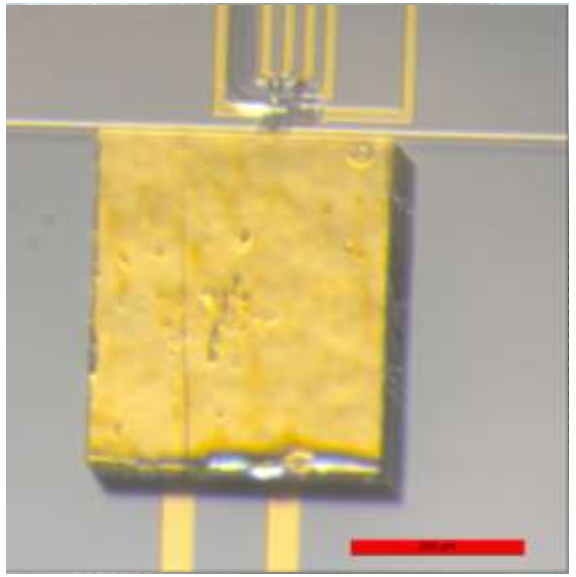
- Pair of electrodes that passes along the edge of the lid.
- Pulses of electrical current, overlapping spot welds.
- All placed inside a chamber with N2

Hermetic sealer PYRAMID

WHAT ABOUT THE LIGHT?







Coupling of the PIC with the light source

1.2. PROCESSES. COUPLING LIGHT BETWEEN DIFFERENT MEDIA

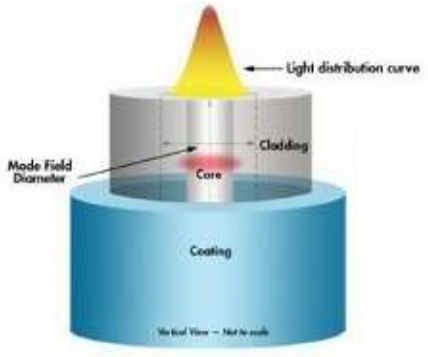
- **MFD Mode Field Diameter**: measure of the width of the light distribution.

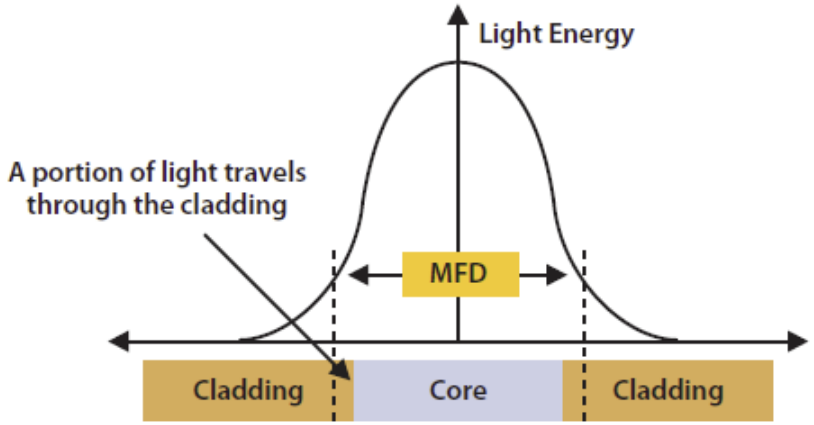
- **Optical coupling:** for efficient transfer of optical energy from one component to another, their respective mode profiles should overlap as much as possible.

  Insertion Loss: efficiency with the power is transferred from one optical component unto another component.

$$IL[dB] = -10\ log_{10}\frac{P_2}{P_1}$$

P_1 = *Input Power*
P_2 = *Output Power*



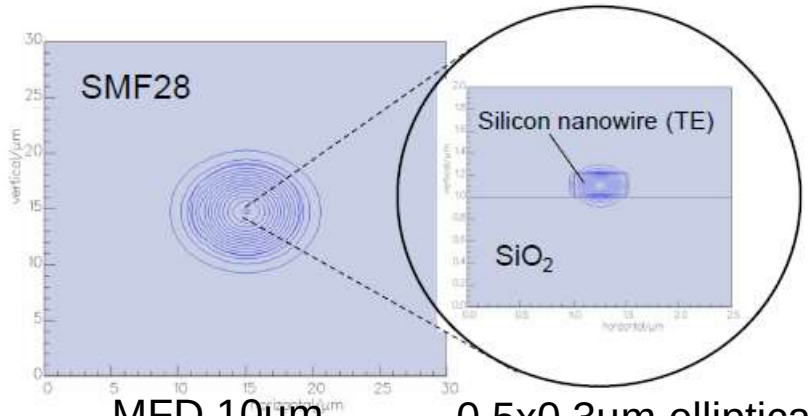


1.2. PROCESSES. COUPLING LIGHT BETWEEN DIFFERENT MEDIA

Fiber to PIC coupling

HORIZONTAL OR EDGE COUPLING: Light beam is coupled in/out from the waveguide from lateral sides.

- ✓ No polarization dependence, broadband.
- ✓ High coupling efficiency (IL≈1dB).
- ✗ Tight positioning tolerances.
- ✗ Requires the realization of optical-quality facets.



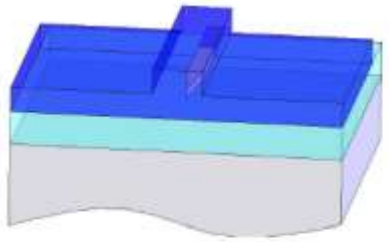
MFD 10µm

0.5x0.3µm elliptical

VERTICAL OR GRATING BASED COUPLING: the light beam is incident from the top surface of the chip.

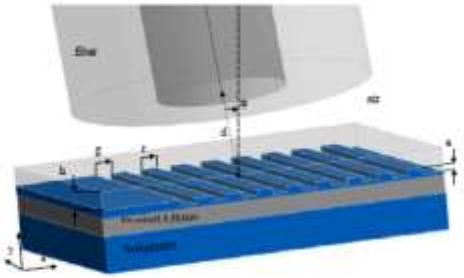
- ✗ Polarization and wavelength sensitivity.
- ✓ Relaxed positioning tolerances
- ✗ Lower bandwidth
- ✗ Lower coupling efficiency. (IL ≈ 3-4dB)
- ✓ Wafer scale testing

Lateral coupling



- typically based on inverted tapers
- spotsize: ~3 µm

Vertical coupling



- typically based on gratings
- spotsize: ~ 10 µm

1.2. PROCESSES. COUPLING LIGHT BETWEEN DIFFERENT MEDIA

ACTIVE TECHNIQUES

The adjustment of the coupling is carried out online by micromechanical actuators and fixed after **optimization of the optical coupling.**

✓ Good light coupling guaranteed.

✗ Time and labor intensive.

✗ High cost.

PASSIVE TECHNIQUES

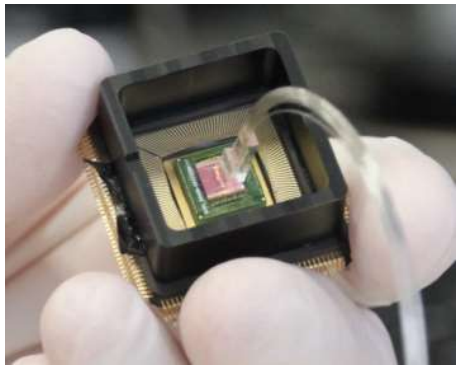
Component **directly attached** to the substrate, high resolution markers.

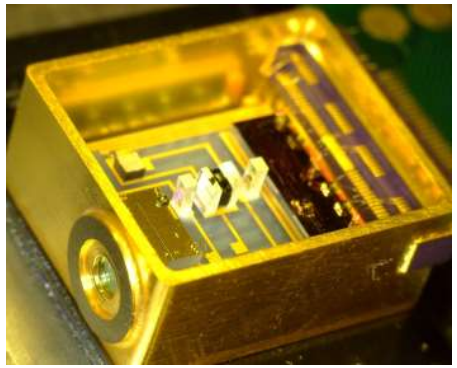
✗ Coupling dependent on the precision in the positioning.

✓ Wafer scale, short times.

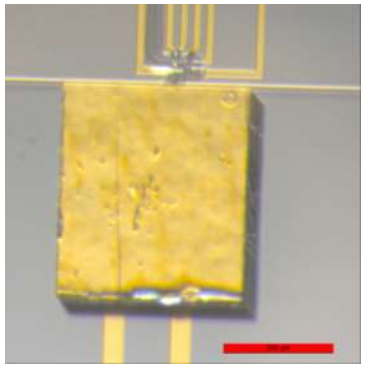
✓ Low cost.

PIGTALING AND FREE SPACE OPTICS





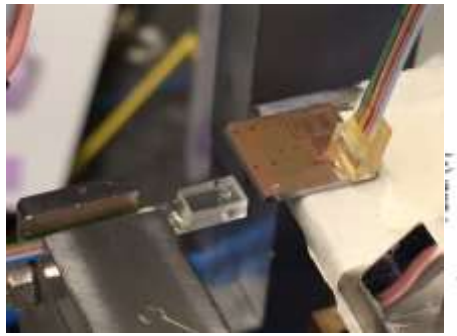
FLIP CHIP – HYBRID INTEGRATION

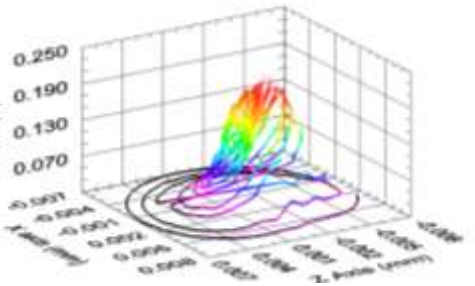


1.2. PROCESSES. COUPLING LIGHT BETWEEN DIFFERENT MEDIA

Pigtailing

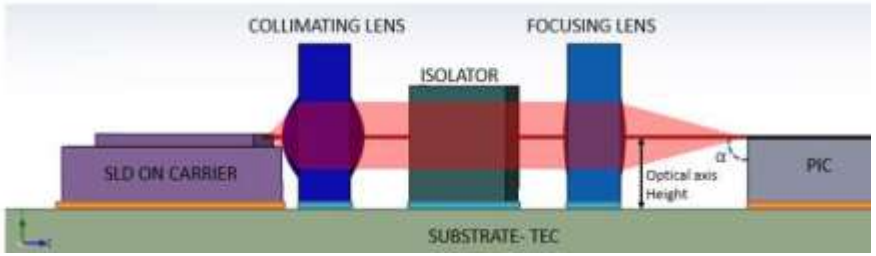
- **Fiber array** attached to the PIC.
- **Horizontal / vertical** fiber coupling.
- **Steps**: Passive pre-alignment + Active alignment (IL minimization) + Fixing UV curable optical epoxy.
- **Active alignment**: external laser + power meter connected to two ending fibers.





Free space optics

- **Microlenses** to adapt the laser mode to the PIC waveguide.
- **Horizontal** coupling.
- **Steps**: Passive pre-alignment + Active alignment (IL minimization) + UV curable optical epoxy.
- **Active alignment**: to maximize current signal revealed from monitor PD previously integrated in the PIC.



1.3. INPHOTEC

INTEGRATED PHOTONICS TECHNOLOGY CENTER

700 m2 cleanroom space
- 40m2 class 100 ISO5
- 190m2 class 1000 ISO6
- 320m2 class 10000 ISO7
- 150m2 service area

6” front-end (upgradable to 8”) + back-end lines

Start operations: Jan 2015

- Unique fab in Italy
- Industry attractive
- Innovative products and efficient services for research and SME

1 | INTRODUCTION TO PHOTONICS PACKAGING
1.3. INPHOTEC

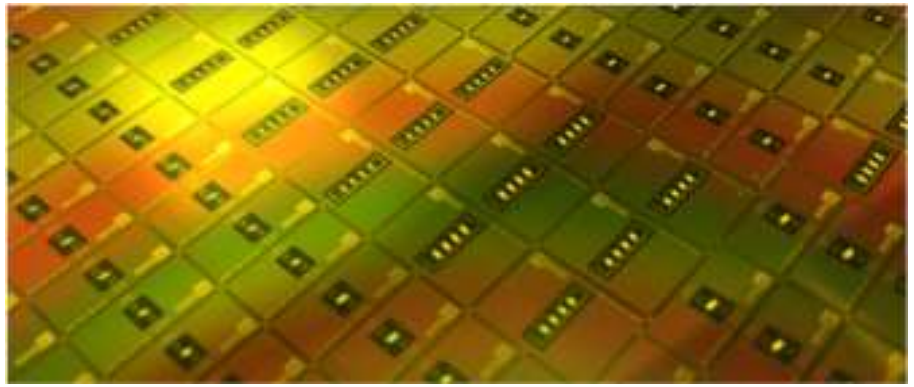
PLATFORM SILICON PHOTONICS
- Passive devices fabrication
- Gratings and SSC fabrication

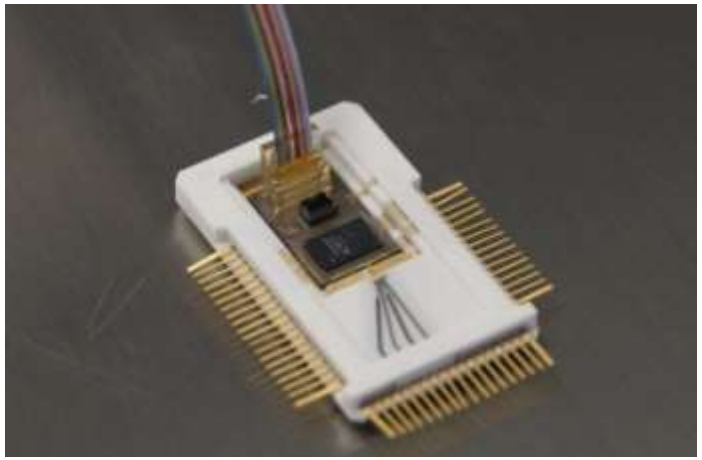
PLATFORM GLASS AND NITRIDE
- SiN passive circuits
- Glass on Silicon passive circuits
- Glass on glass passive circuits

PLATFORM HYBRID INTEGRATION
- Metallization for pads, routing
- Gold/tin solder deposition
- Deep Etching

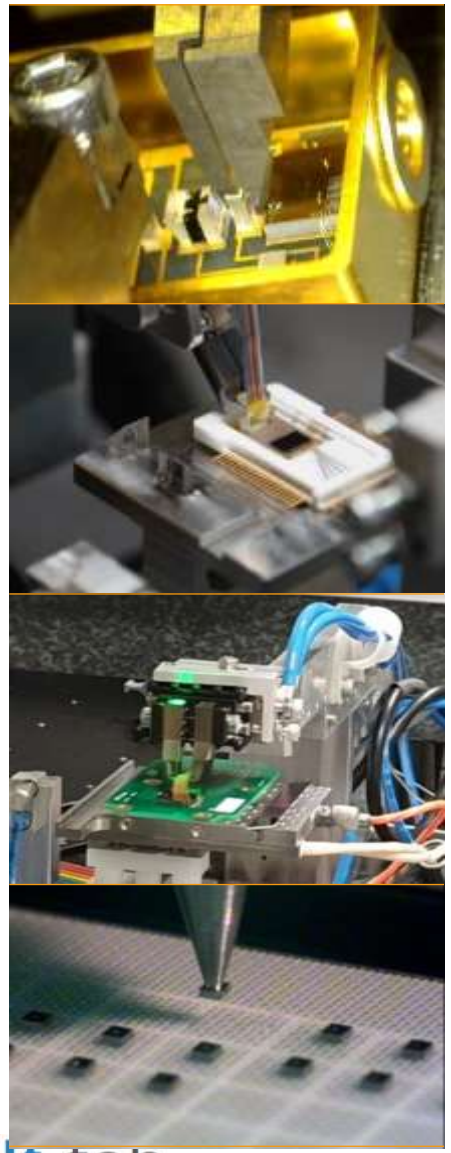
PLATFORM ADVANCED PACKAGING
- Die attachment soldering
- Wire bonding interconnections
- Pigtailing (edge and gratings) or lenses alignment
- Flip chip for submicron attachments
- On board packaging, flex cables soldering
- 3D packaging
- Hermetic enclosures

6” Si wafer





1.3. INPHOTEC. ADVANCED PACKAGING PILOT LINE



Optical connections – Active alignement pigtailing

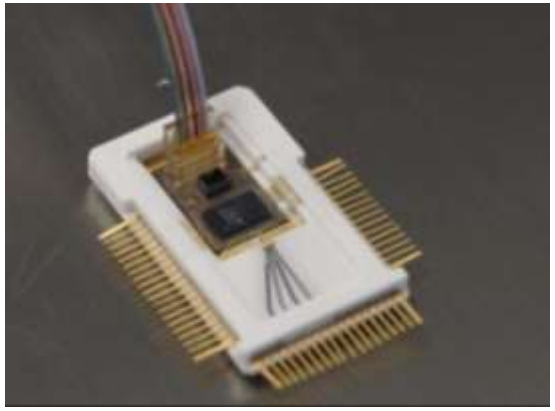
- Vertical (GC) and horizontal (SSC) alignment to fibers, interposers and waveguides (Si, SiN, SiO2, III-V…)
- Micro-lens alignment and attachment

Electrical connections – Chip & wire assembly

- Die-attach and Flip-Chip Bonding
- PIC/EIC integration (3D stacking)
- Tacking, In situ reflow, Eutectic bonding, laser assisted soldering
- Gold Stud bumps deposition and thermocompression bonding
- Flux less / solder paste / void free soldering
- Wire and ribbon bonding with glob-top
- Hermetic housing

1 INTRODUCTION TO PHOTONICS PACKAGING
1.3. INPHOTEC. ADVANCED PACKAGING PILOT LINE

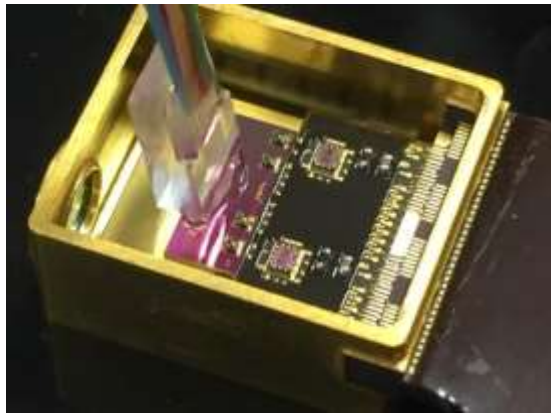
Automation



Pre-production for qualification tests (10^2 - 10^3 pcs) of commercial transceiver device:

- Si photonics based
- 16 optical and 90 electrical connections (DC + RF)
- Laser MicroPackage integration (active alignment)

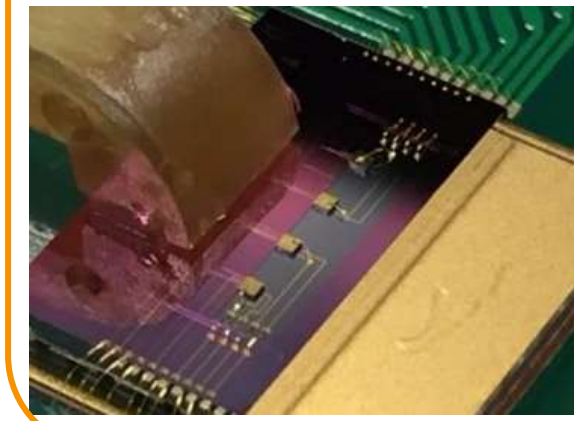
Radio Frequency



RF signal management from the PIC to the PCB:

- Ceramic interposer
- Short wire bondings
- Housing
- Flex soldering

III-V Chip integration



- Hybrid integration of SOAs
- Sub-micron passive alignment of LD/SOA
- Thermal management (TEC)
- Chip on board assembly

High reliability applications

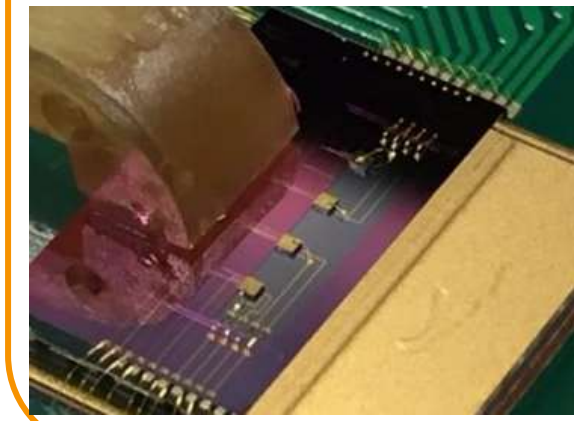
esa
European Space Agency

Certified ph packaging for space – ESA PIOTS project

Prototipation and production of packaged PIC devices (up to thousands pcs/year), in line with ISO 9001-2015 and ESCC/ECSS full standards compliance.
(Project duration 2019-2021)

2. Hybrid Integration of Si Ph Devices

III-V Chip integration



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2 | HYBRID INTEGRATION OF SI PH DEVICES
2.1. MOTIVATION

Si Photonics

- Ideal material for integrated optics
- Highly integrated & low-cost optical components
- Based on CMOS manufacturing techniques
- Main platforms: SOI, SiN, Glass on Si.
- Lack of a direct bandgap.
- Devices: laser cavity, waveguides…

III-V Compounds

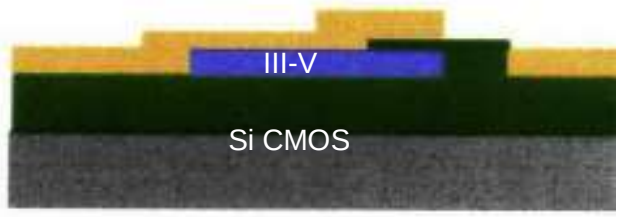
- Direct bangap: active devices
- High cost.
- Main platforms: GaAs, AlGaAs, InP.
- Devices: laser, photodetectors, SOA...

Si Ph + III-V DEVICE INTEGRATION

2.2. HYBRID vs MONOLITHIC INTEGRATION

MONOLITHIC INTEGRATION

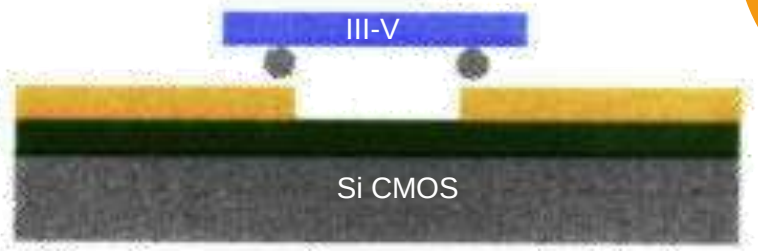
- Components made of the same material “of a piece”.
- Integrate III-V layers on a Si Ph wafer by direct epitaxial growth.
- Technological challenging.
- Mechanical robustness: no additional interfaces.
- Low yield.



HYBRID INTEGRATION

- Fully process Si Ph and III-V chips separately, followed by placement of individual III-V die onto the Si.
- Flip chip bonding.
- Lower mechanical reliability because of many electrical and optical interfaces.
- Requires very precise alignment.
- High yield -> preferred in industry

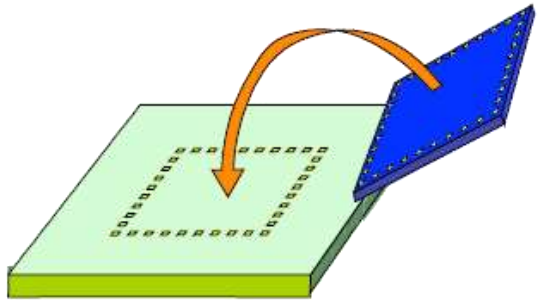
FLIP CHIP BONDING



2 | HYBRID INTEGRATION OF SI PH DEVICES
2.3. FLIP CHIP BONDING.

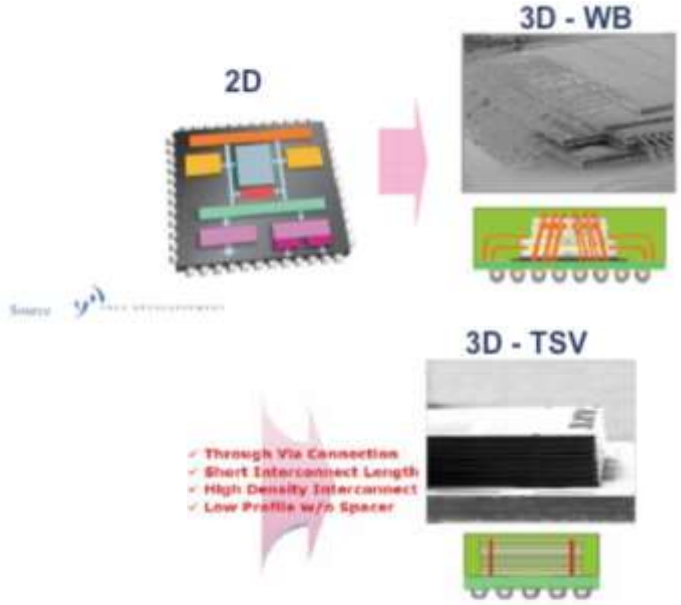
What is?

- Direct attachment of chips to a substrate (chip, package, PCB…) with the chip surface facing the substrate.
- Developed in 1964 by IBM with the aim **to replace wire bonding** method.



Why?

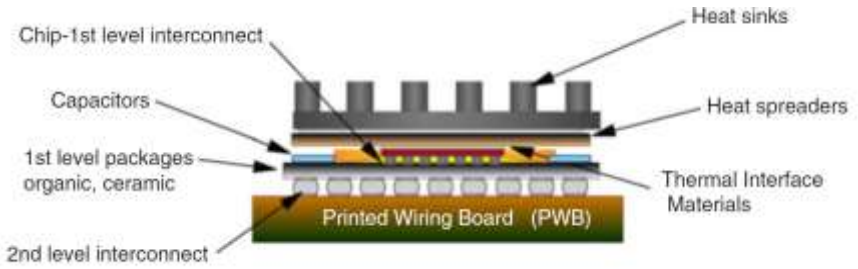
- Highest number of I/O
- Very high component density (smallest footprint)
- Low profile and small physical area (small packages)
- Best electrical performance (shortest interconnection)
- High frequency performance
- Low cost



2 HYBRID INTEGRATION OF SI PH DEVICES
2.3. FLIP CHIP BONDING.

Where?

- First – second level packaging
- Die to die: EIC + PIC systems, III-V + Si Ph devices
- Package to package



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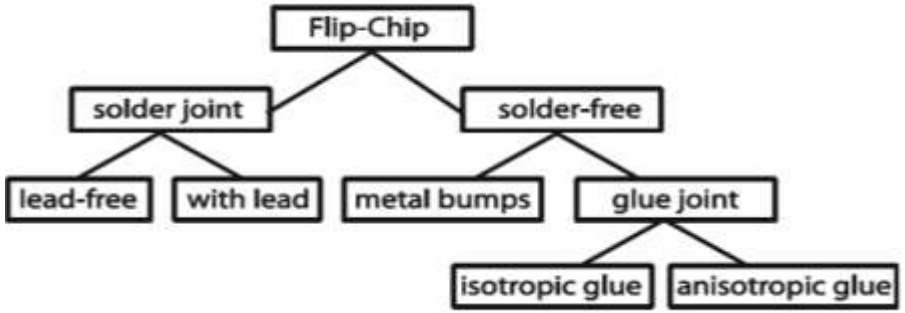
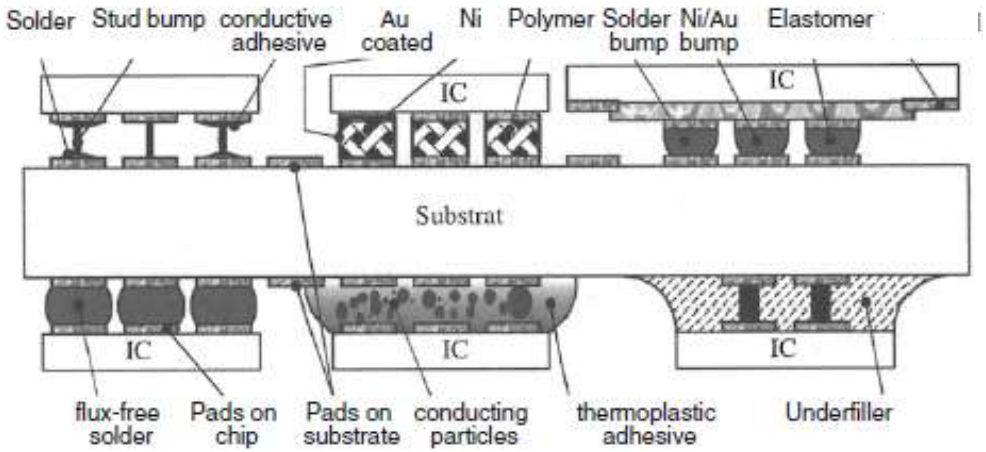
How?

- Electrical and mechanical connections are realized through conductive **micro bumps** e.g. solder bumps and gold studs.
- Other connecting materials:





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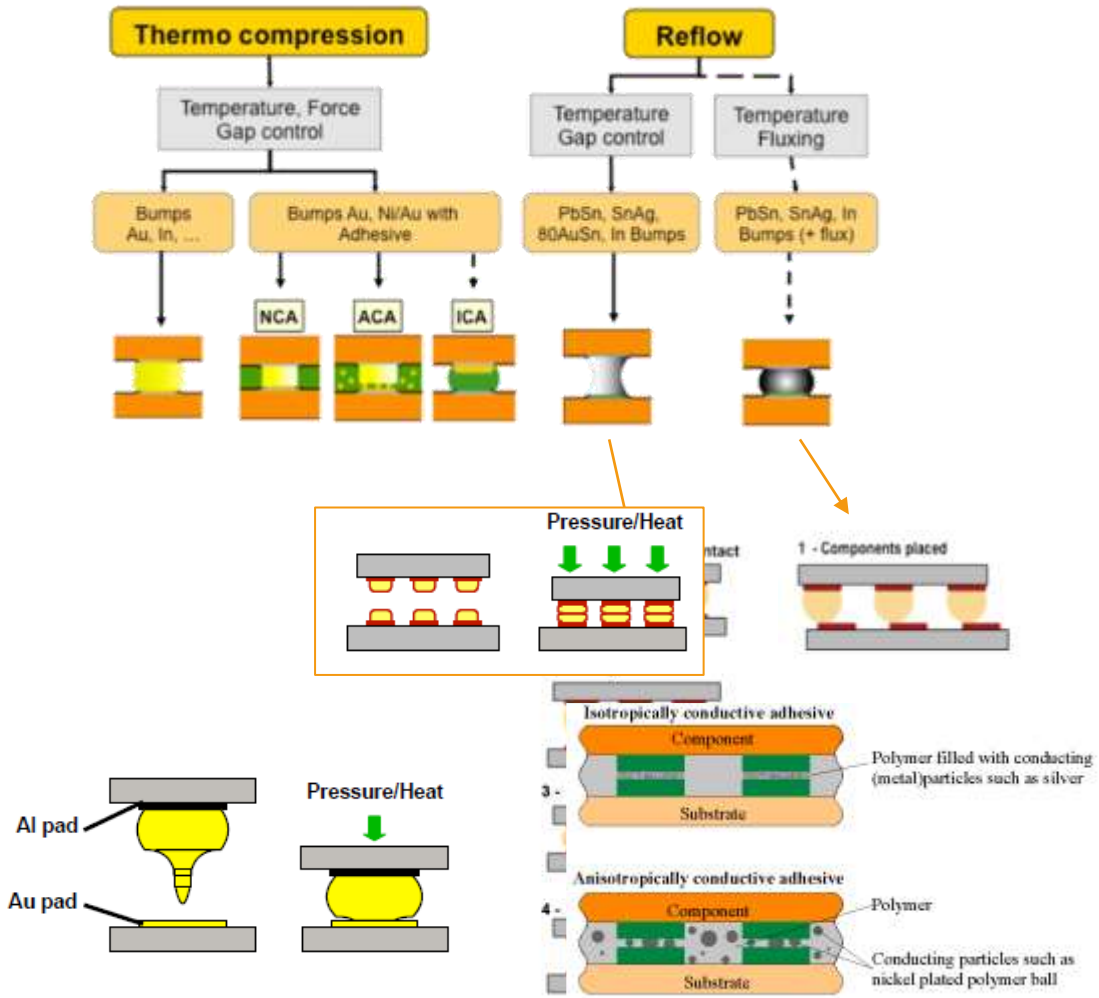
2.3. FLIP CHIP BONDING. METHODS OF JOINING



THERMOCOMPRESSION: The bumps of the chip are bonded to the pads on the substrate by force and heat.

- **Au Stud bumps, AuSn solder bumps.**
- **Adhesive bonding:** bumps + adhesive.
  - **NCA**: Non Conductive. Joint surfaces into contact.
  - **ACA**: Anisotropic Conductive. Filled epoxy, electrical insulation before bonding, electrically conductive in Z-direction after bonding
  - **ICA**: Isotropic Conductive. Filled epoxy, conductivity in all directions.

REFLOW. Solder bumps.

- **Solder mass reflow**: self-alignment. The molten solder starts wetting the metal pad and moving the chip by surface tension force.
- **In-situ relfow:** joint shaping.

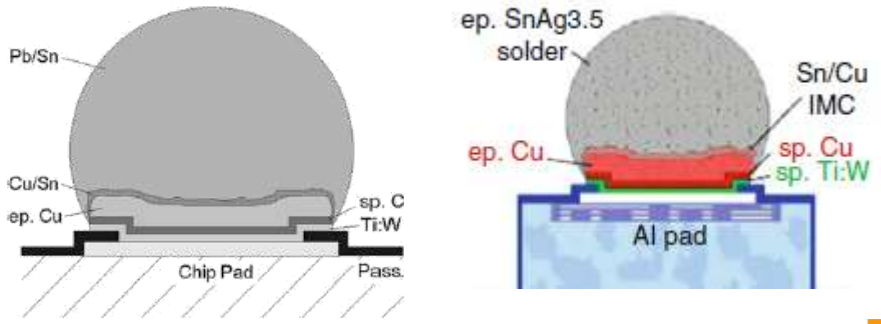
2 HYBRID INTEGRATION OF SI PH DEVICES
2.3. FLIP CHIP BONDING. BUMPS MATERIALS

Bumps based on soft solders

- MOST COMMON FOR ALL **MICROELECTRONIC** SYSTEMS
- Possibility of **repair.**
- **Solder mask,** o avoid the flow of the solder over the whole surface.
- When CTE mismatch between chip and substrate: **UNDERFILLER** (epoxy).
- **Reflow process** (+10ºC higher than theoretical melting point)
- **Flux:** oxidation.

Table 3.4 Selection of solders for flip-chip interconnects

Solder	Melting point	Remark
63Pb37Sn	183 °C	Eutectic PbSn, low melting point, compatible with organic PCBs, commonly used for most SMDs. Not allowed anymore for ROOS
95Pb5Sn (or similar)	315 °C	High-lead, good electromigration behavior, highly reliable thermo-mechanical interconnect, flip chip on ceramic substrate; no reflow of high lead bumps during chip attach on PCB (eutectic PbSn on PCB side), flux free reflow in H_2 atmosphere
96.5Sn3.5Ag (or similar)	221 °C	Currently most common binary lead free solder for flip chip. Typically used in conjunction with electroplating
97Sn/3Cu	227 °C	Difficult to electroplate. Short bath lifetime
95.5Sn3.9Ag0.6Cu	218 °C	Common lead-free solder paste, Cu content reduces Cu consumption from UBM
80Au20Sn	280 °C	Common for flux free opto-electronic assembly on gold finishes, controlled standoff height
In	157 °C	Ideal for temperature sensitive electronic devices due to very low reflow temperatures
Sn	232 °C	Risk of tin whisker formation

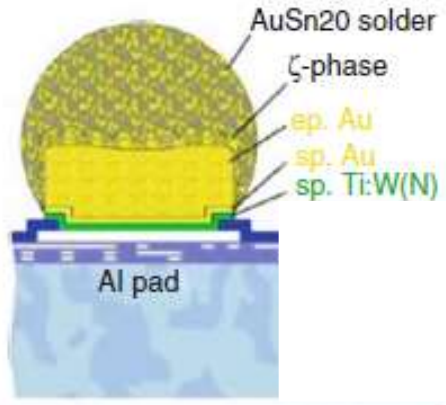


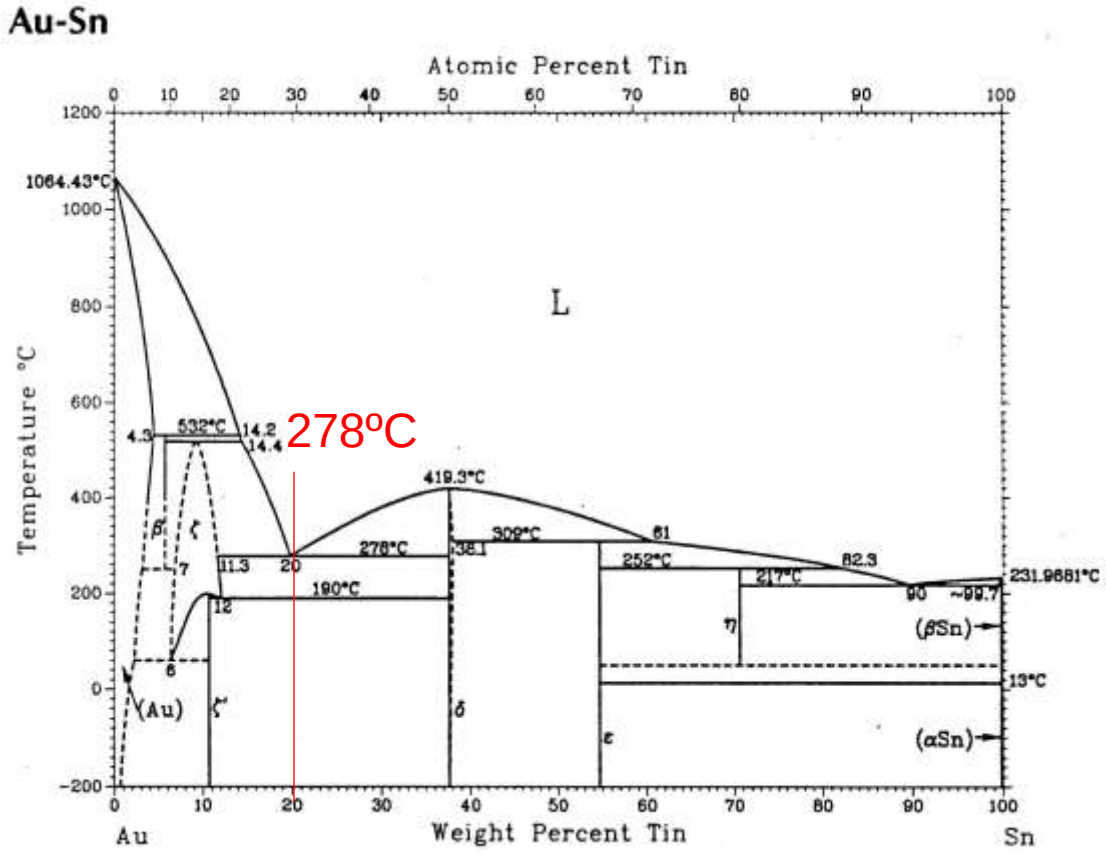
DOI 10.1007/978-1-4419-5768-9

2.3. FLIP CHIP BONDING. BUMPS MATERIALS

Bumps based on AuSn

- MOST SUITABLE INTERCONNECTION MATERIAL FOR **OPTICAL AND OPTOELECTRONIC** DEVICES.
- Good **corrosion** resistance
- **Flux-less** soldering processes: avoiding contamination of the optical components.
- **Eutectic**: Au80Sn20 (melting point 278ºC)
- Good **mechanical** properties





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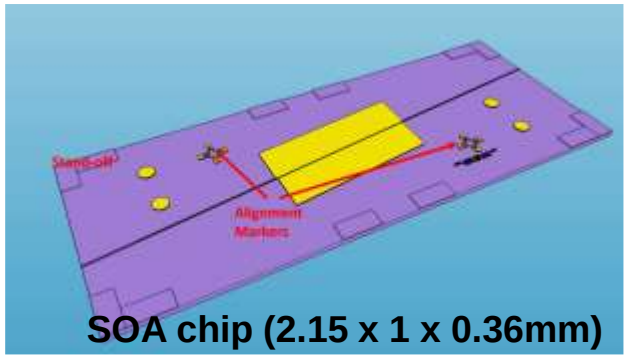
WHAT ABOUT THE LIGHT?

Laser to PIC coupling

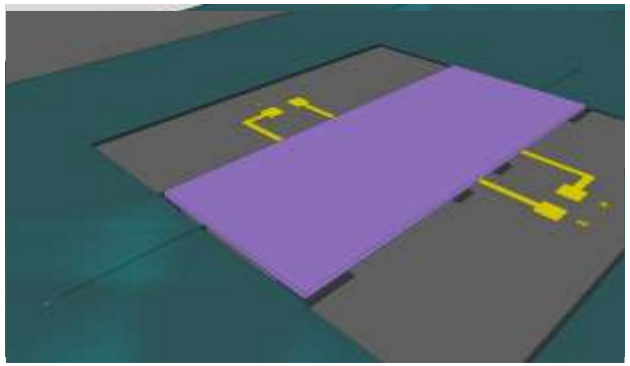
2.4. A REAL CASE – SOA INTEGRATION

SOA INTEGRATION IN SI PHOTONICS
EXTERNAL CAVITY LASER

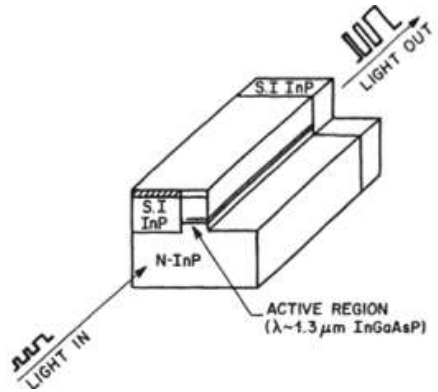
FLIP CHIP BONDING III-V SOA + SOI PIC



SOA chip (2.15 x 1 x 0.36mm)



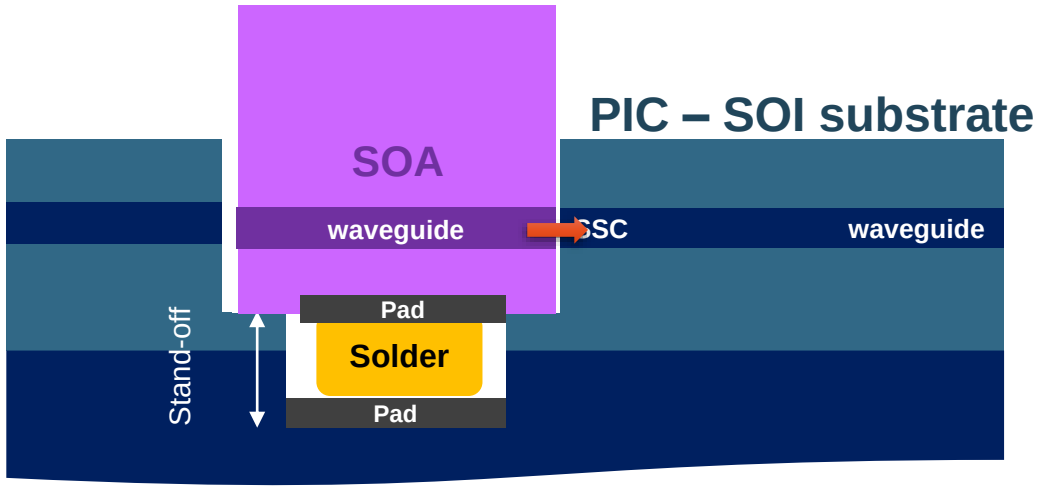
- SOA= Semiconductor Optical Amplifier
- Is a device that providing an **external electrical current**, **amplifies** an incident light.
- Light is amplified when it propagates through a semiconductor gain medium fabricated in the form of a **waveguide**.

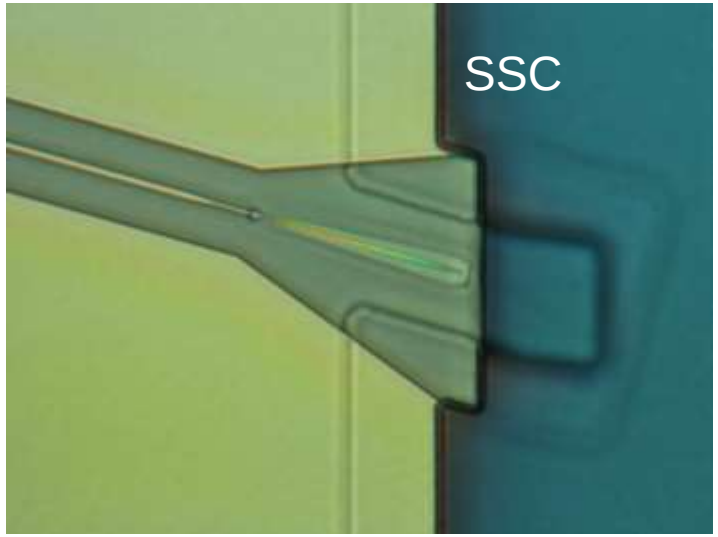


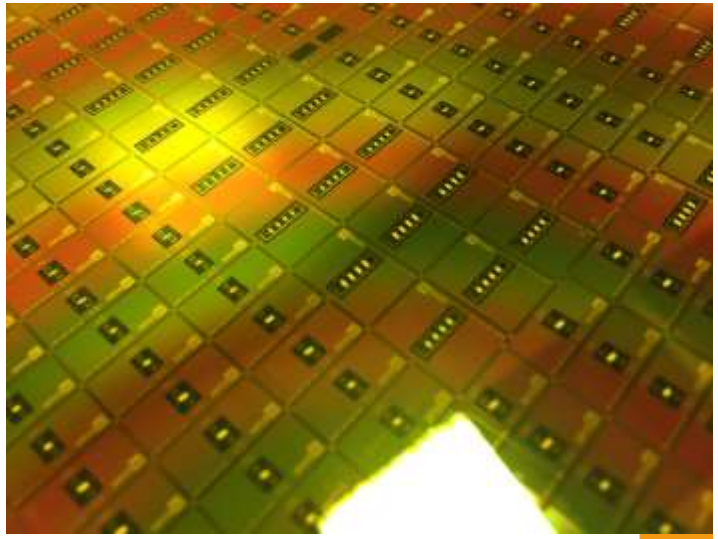
2.4. A REAL CASE – SOA INTEGRATION

- **OPTICAL I/O :** Horizontal or edge coupling.
  - MFD mismatches: Design of SSC with MFD =3-4µm compatible with SOA waveguide.
  - Low Insertion Loses: <1µm placement accuracy.

- **ELECTRICAL I/O:** flip-chip bonding aided by $Au_{0.8}Sn_{0.2}$ solder deposition (e-beam evaporation) – 6-inch wafer.



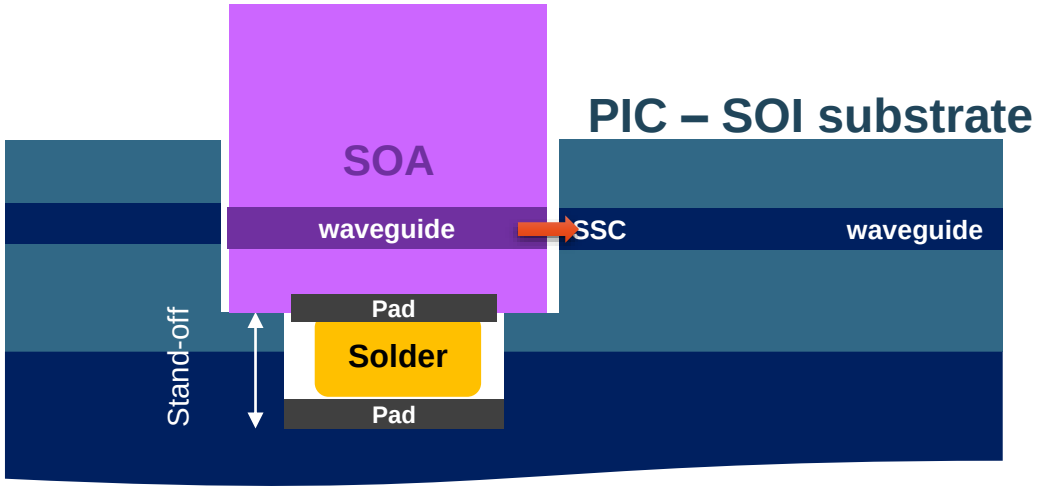


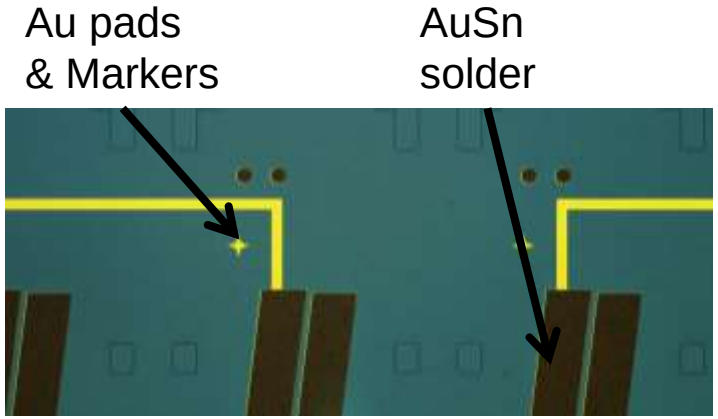


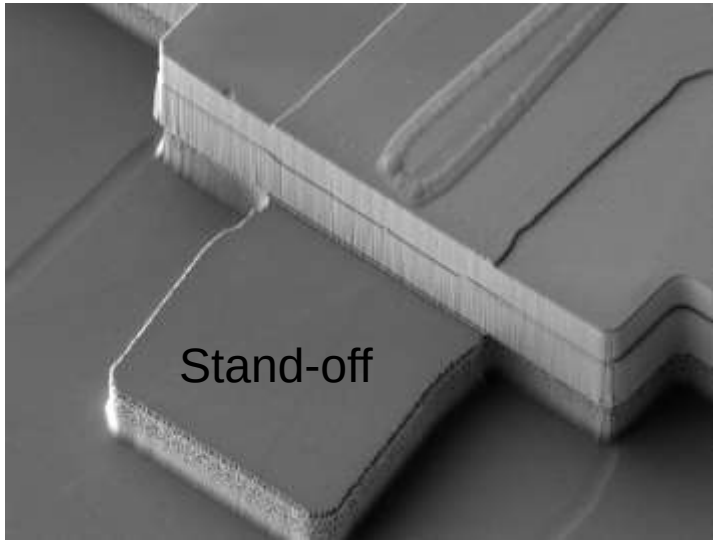
2.4. A REAL CASE – SOA INTEGRATION

- **IN PLANE ALIGNMENT (XZ):** Lithography-defined fiducials for sub-micron accuracy flip-chip bonding.

- **OUT-OF-PLANE ALIGNMENT (Y):** substrate cavity + reference stand-off.







2.4. A REAL CASE – SOA INTEGRATION. DIE BONDER

Characteristics

- Accuracy **down to ±1µm** @ **3s** while bonding with temperatures >350ºC.
- Eutectic bonding via **diode-laser or heating plate**.
- Cycle-times down to **25 sec** AuSn eutectic process.
- Small die size down to 100um.
- Bond force control.
- Supports all **dispensing** technologies.
- Full automatic process: Image processing systems – **pattern recognition**.

2.4. A REAL CASE – SOA INTEGRATION. DIE BONDER

Key elements

LASER SOLDERING

- Highly **localized melting** of the solder joint.
- **Wafer level process** (12”): no thermal crosstalk between the different chips.
- Mechanically and electrically stable connection when solidified.
- Laser diode, λ 808nm.

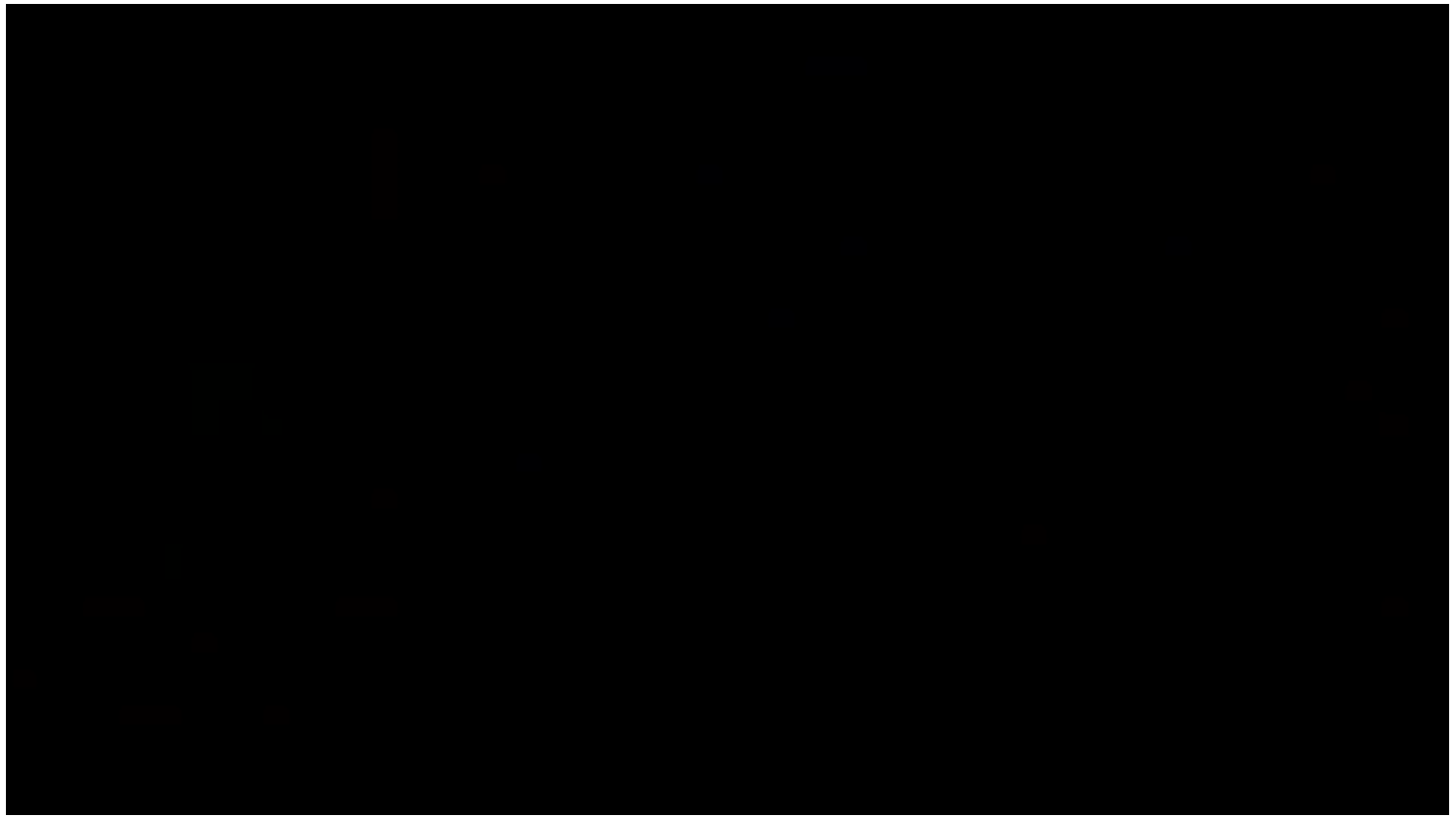
PATTERN RECOGNITION

- Fully **automatic** passive process.
- Placement **accuracy <1um**.

2.4. A REAL CASE – SOA INTEGRATION. DIE BONDER

PROCESS

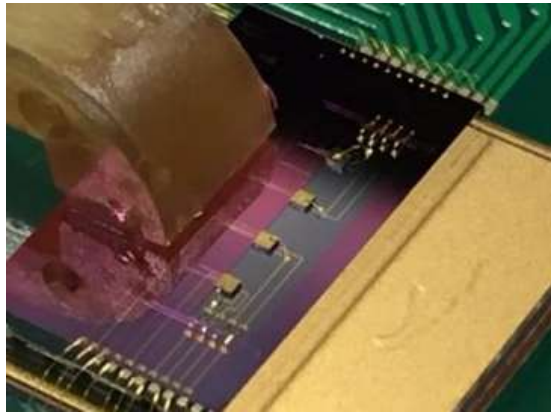
1. **COMPONENTS IN**
   - Gelpack with dies
   - Wafer or substrate
2. **LOADING** – Bonding head pick up die.
3. **ALIGNMENT** – die & substrate markers
4. **PLACEMENT** – of the die on the substrate
5. **BONDING** – heat up to melt solder
6. **POST-BONDING** ANALYSIS – precision of the final die position
7. **POPULATED WAFER OUT**



https://www.youtube.com/watch?v=39FU9ygmzcU&ab_channel=ASMAMICRAMicrotechnologies

3. PHOTONICS PACKAGING FOR SPACE APLICATIONS

III-V Chip integration



- Hybrid integration of SOAs
- Sub-micron passive alignment of LD/SOA
- Thermal management (TEC)
- Chip on board assembly

High reliability applications

esa
European Space Agency

Certified ph packaging for space – ESA PIOTS project
Prototipation and production of packaged PIC devices (up to thousands pcs/year), in line with ISO 9001-2015 and ESCC/ECSS full standards compliance.
(Project duration 2019-2021)

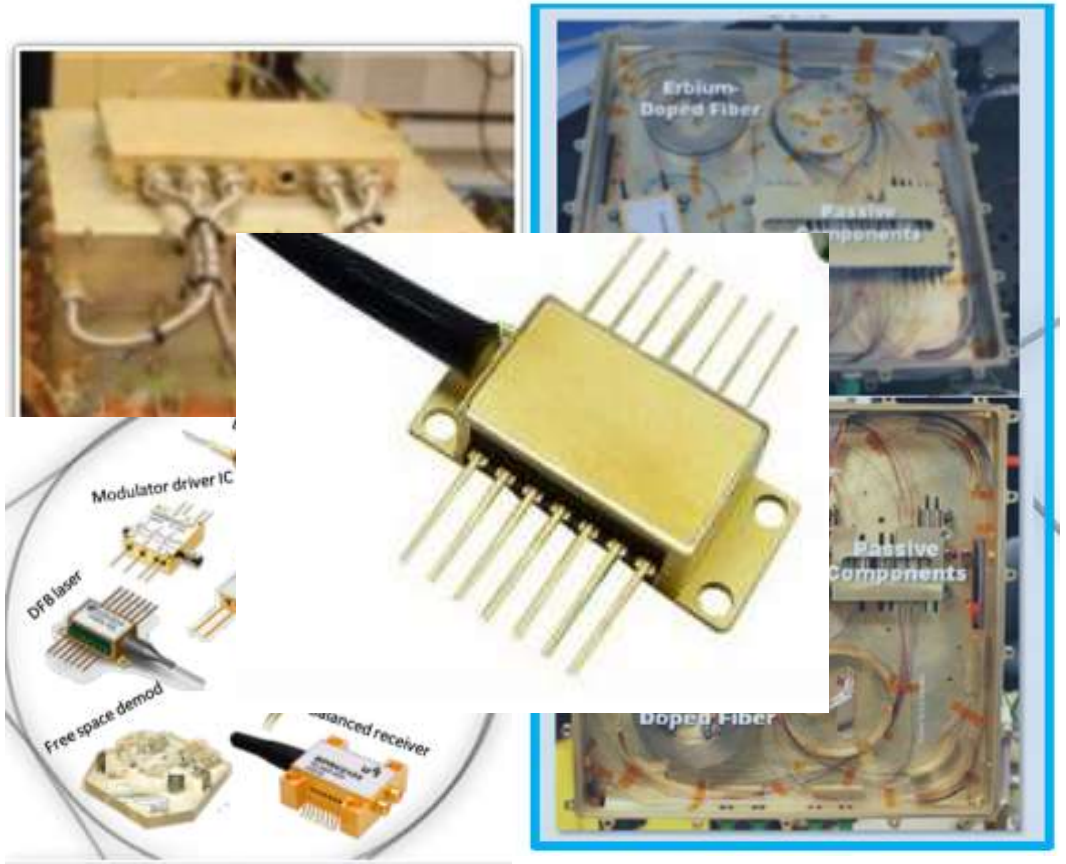
3 | PHOTONICS PACKAGING FOR SPACE APPLICATIONS

Advantages of Integrated Photonics

- **SWAP: Size, Weight and Power reduction.**
- Removal/reduction of **electromagnetic interferences.**
- Convergence with integrated electronics with potential **costs reduction and improved performance**.
- Possibility to avoid optical to electronic to optical conversions by maintaining some functions at **photonic level** in the optical domain.

EIC + PIC + LASER integration

State of the art: space compliance modules based on discrete devices manually assembled.



3 PHOTONICS PACKAGING FOR SPACE APPLICATIONS

LIMITING FACTOR TO EXPLOTATION OF INTEGRATED PHOTONICS IN SPACE APPLICATIONS

Space Compliance Integrated Ph Packaging Technologies

- ECSS: European Cooperation for Space Standardization.
- ESCC: European Space Components Coordination
  - ESCIES: European Space Components Information Exchange System
  - EPPL: European Preferred Parts List

ESCC 2566000

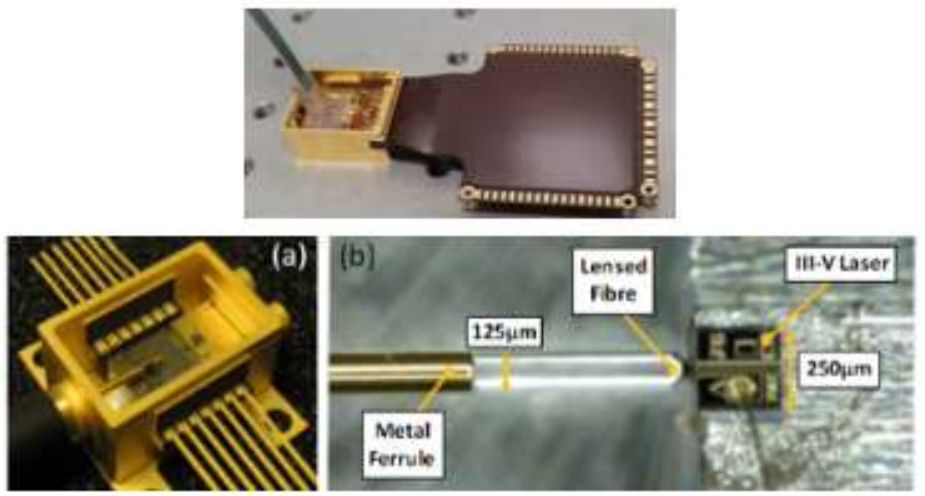
Requirements for the process capability approval for manufacturing lines of Hermetic Hybrid Microcircuits for space applications.

Open points to be solved:

PIC – LASER INTEGRATION.
Necessity of multiple fiber I/O

MULTI CHANNEL HERMETIC OPTICAL IN-OUT
State of the art: Multi-channel non-hermetic / One-channel hermetic

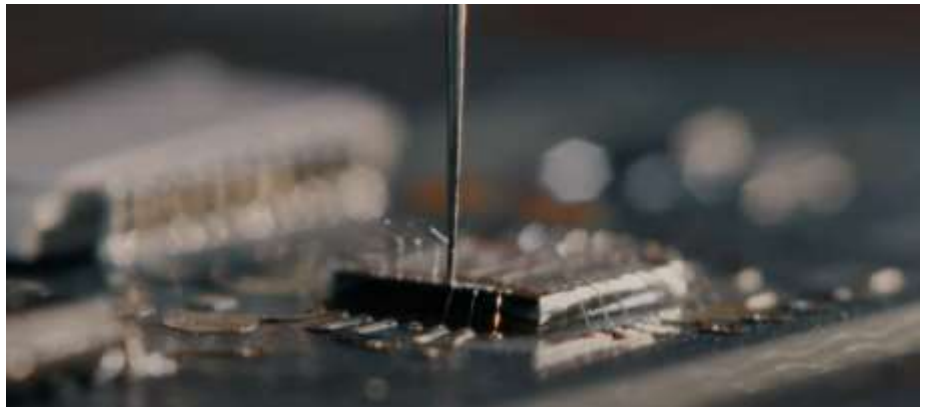
QUALIFICATION OF TEST VEHICLES
MIL-STD-883 Test Method Standard – Microcircuits.
United States Department of Defense Standards



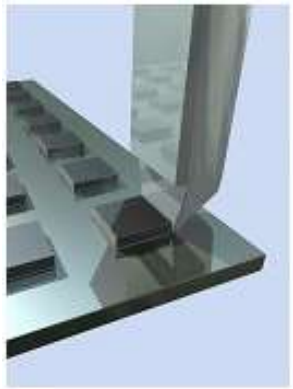
3 PHOTONICS PACKAGING FOR SPACE APPLICATIONS

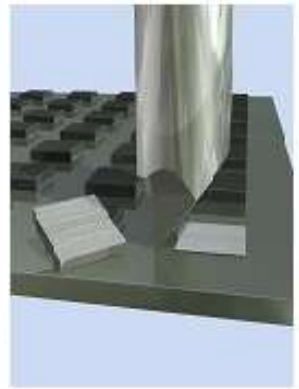
N°	Test	MIL-STD	Method	Test conditions and remarks
				system, between conductors on same layer in a monolayer system
16h	SEM Inspection	883	2018	Provide photos of typical assemblies, non conformances and anomalies
16i	Bond pull test	883	2011	On TVE2 only. Pull all wires and ribbons
16j	Die shear test	883	2019	On TVE2 only. Shear all chips and small substrates
16l	Substrate attach strength	883	2027	When shear test cannot be performed in case of substrates or large chips
16m	Adhesion test	-		Peeling test on metallization according to the hybrid manufacturer specification and agreed by ESCC executive
16n	Micro-sections	-		Micro-sectioning shall be performed to evaluate : multilayer substrates (conductors, dielectric, vias), assembly of added-on parts, cross-overs, local encapsulations, hermetic sealing (seal joint and feed-through).
17	Solderability	202	208	Three terminals per test item
18	Soldering heat	883	2036	Visual inspection (x 30 minimum) to verify that terminals, glass seals, connections or substrate are not damaged. Conditions as per test method to be defined according to application.
19	Terminal strength	883	2004	Flexible leads : condition A, F (N) = 30 x S (mm²) (F : strength, S : lead section) Rigid feed-throughs in packages : • Diameter ≤ 1mm as above • Diameter > 1mm, condition C1, torque :1,5 N.cm

BOND PULL TEST of wire bonds



DIE SHEAR TEST of all attached chips and substrates

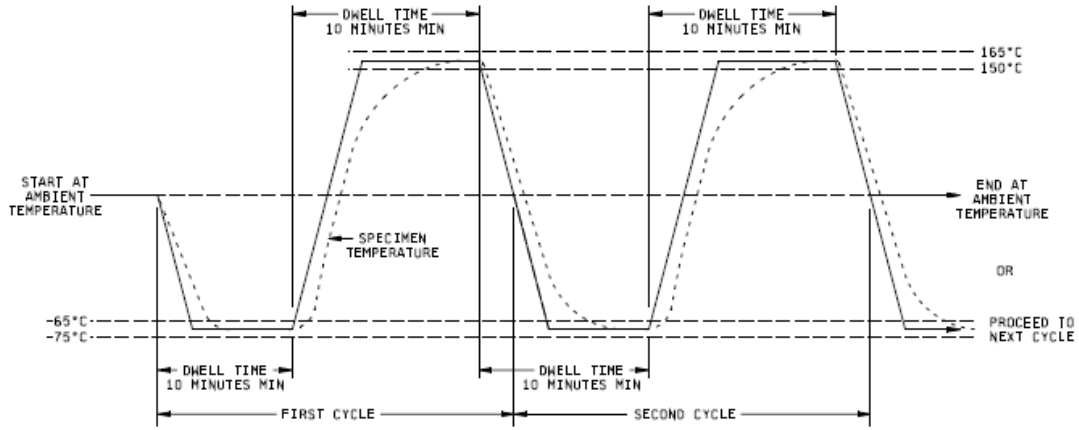




3 PHOTONICS PACKAGING FOR SPACE APPLICATIONS

N°	Test	MIL-STD	Method	Test conditions and remarks
1	Thermal cycling	883	1010	Condition B, 100 cycles per step up to 500 or failure
2a	Endurance	883	1005	Duration 1000h + 1000h. Ambient temperature will be defined to achieve 125°C≤T_j≤150°C (or maximum ratings). If the Tj of the most stressed part is lower than 125°C, the time shall be increased according to MIL-STD-883 Method 1005.
2b	High Temperature Storage	883	1008	Condition B: +125°C; 2000 hours
3	Mechanical shock	883	2002	Step1 : Condition B (1500g) for packages up to 1" x 2" and 1000 g 0,5 ms for packages above. Step 2 : Condition C (3000g) for packages up to 1" x 2" and Condition B (1500g) for packages above. Shocks performed on Y1, Y2, X and Z axes
4a	Random vibration	883	2026	Condition I K, Random Vibration 44.8 g RMS, 3 axis
4b	Sinusoidal vibration	883	2007	Condition B, 50 g
5	External Visual Inspection	883	2009	
6	Thermal vacuum			20 cycles -30 + 70 °C at 10-5 Pa, dwell time : 2 hours, slope 2°C/minute
7	Burn-in simulation			Bake during 240 h at 125 °C, no voltage
8	Resistance to solvents	883	2015	ESCC 24800 may be used instead of the MIL Method
9	Moisture resistance	883	1004	10 V DC between all terminals connected together and

TEMPERATURE CYCLING: resistance to extremes high and low temperatures, and the effect to alternate exposures to these extremes.



RANDOM AND SINUSOIDAL VIBRATION: resistance to dynamic stress.

N°	Test	MIL-STD	Method	Test conditions and remarks
				package (+ on terminals)
10	Internal Visual inspection	883	2017	Class K requirements
11	Physical dimensions	883	2016	According to test vehicle detail specification. e.g. for TVE1 : line width, space, vias diameter, substrate camber,… e.g. for TVE2 : external dimensions, lid and package deformation,…
12	Electrical measurements ient of resistance			As per TVE2 specification
13	PIND test	883	2020	Condition A. Only applicable to cavity type devices
14	Leak test	883	1014	Fine leak : condition A Gross leak : condition C Only applicable to hermetically sealed, cavity type, devices
15	- None-			
16	DPA (initial or final)			Note 1, Note 2
16a	External Visual inspection	883	2009	
16bc	Radiography	883	2012	When soldered items or gold wires are present
16c	SAM inspection	883	2030	May be used in substitution of radiography
16d	Residual gas analysis	883	1018	
16e	Delidding	883	5009	Micromilling is allowed
16f	Internal visual inspection	883	2017	Class K
		883	2010	Condition A. Or ESCC equivalent for monolithic devices
		750	2072	
		750	2073	
		750	2074	
		883	2032	

LEAK TEST – HERMETIC SEALING

FINE LEAK TEST.
Determines if the leak rate of helium after pressurization is below a rate specified with reference to the package size.

GROSS LEAK TEST.
The package is immersed in a heated fluorocarbon. If a leak exists in the seal periphery, visible gas bubbles will form.

4 CONCLUSIONS

- Importance of Integrated Photonics and packaging of PIC.
- Main technologies involved in PIC packaging: laser / fiber coupling to PIC.
- Hybrid integration III-V semiconductor + Si Ph integration.
- Flip chip bonding technologies, real case app: SOA integration
- Importance of integrated photonics in space applications
- Challenges of the Space Compliance Photonics Packaging Technologies

Thank you!

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