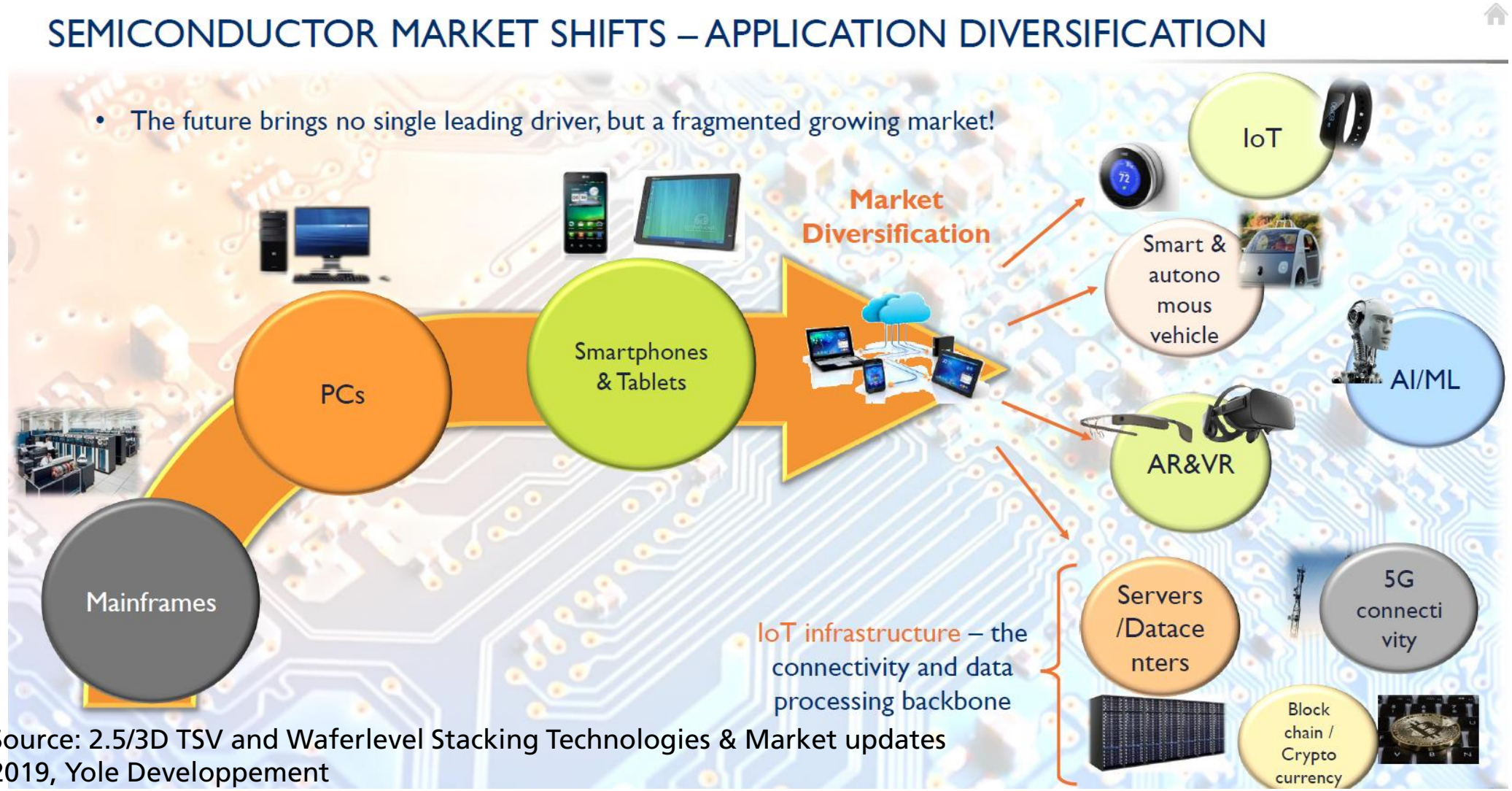
High-density W-filled TSVs for advanced 3D-Integration

Josef Weber

Fraunhofer EMFT, Munich

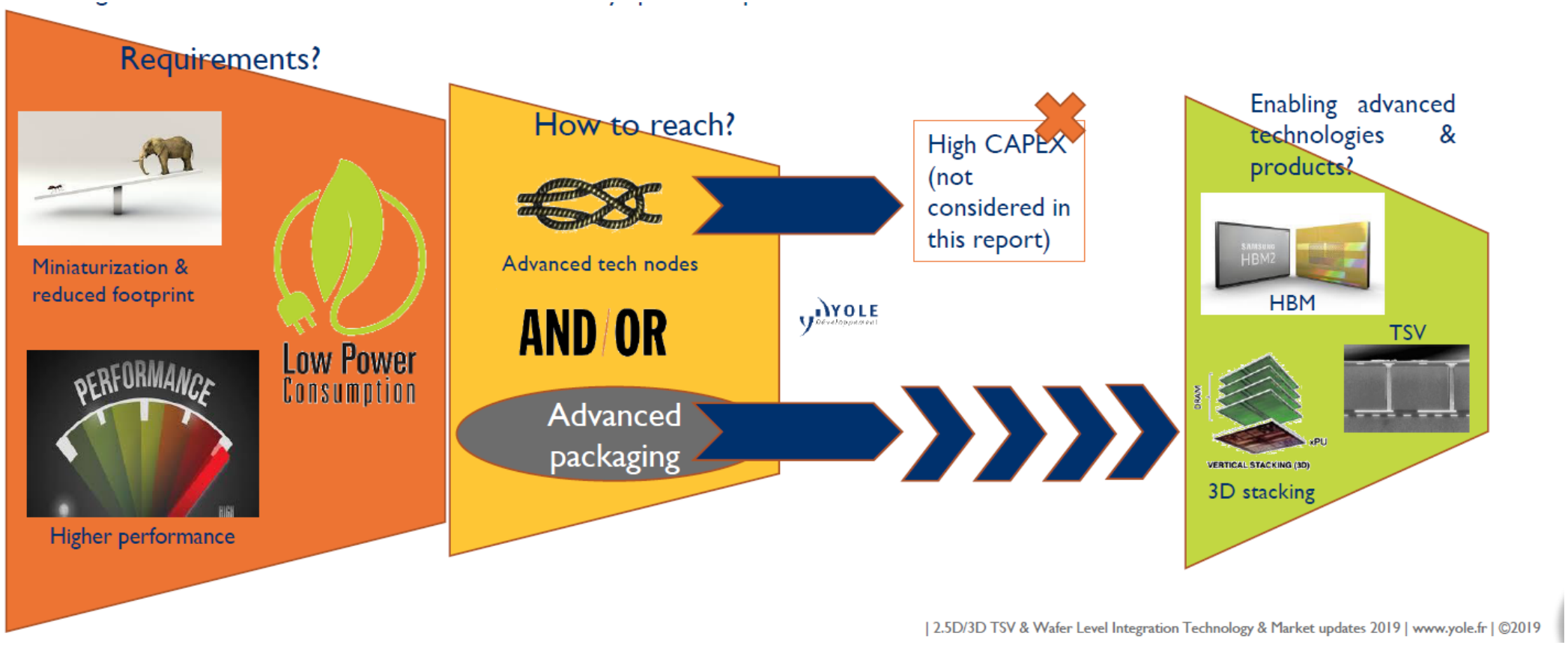
It-fab Italian Network for Micro and Nano Fabrication

Semiconductor Market Application Diversifaction



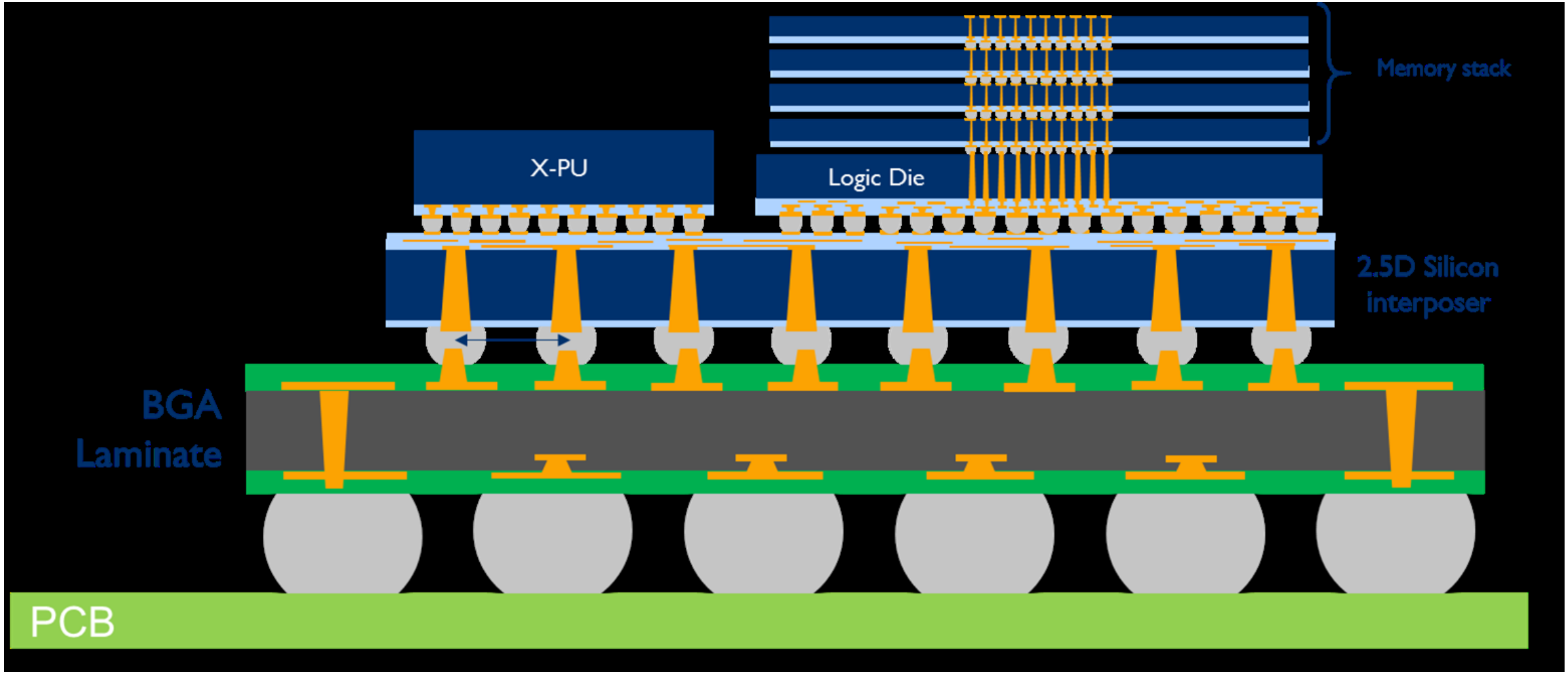
Source: 2.5/3D TSV and Waferlevel Stacking Technologies & Market updates 2019, Yole Developpement

Requirements for Semiconductor and Packaging



Source: 2.5/3D TSV and Waferlevel Stacking Technologies & Market updates 2019, Yole Developpement

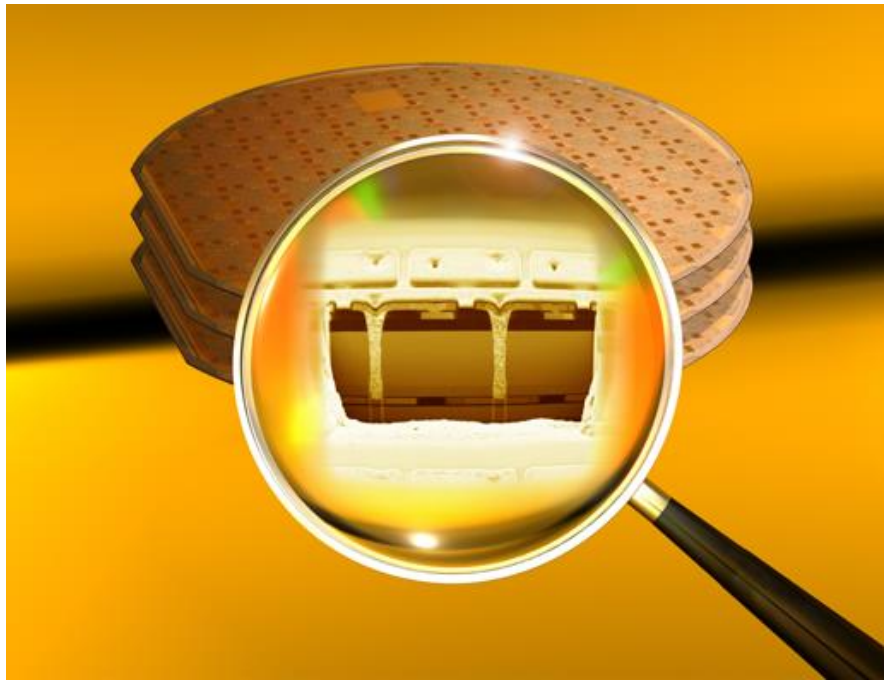
Sketch of typical heterogeneous 2.5/3D-Integration



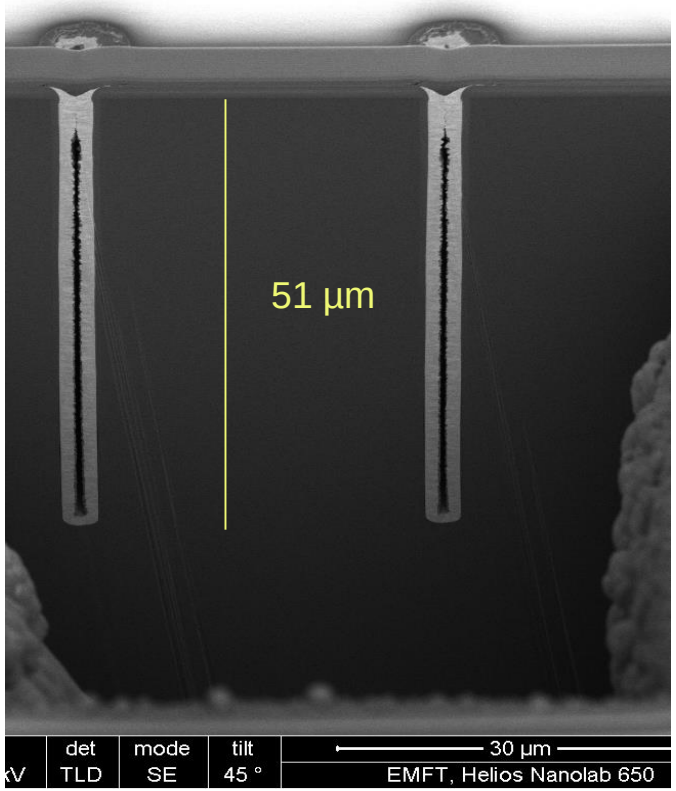
Source: 2.5/3D TSV and Waferlevel Stacking Technologies & Market updates 2019, Yole Developpement

3D - TSV Integration at Fraunhofer EMFT

3D-TSV-Integration on Wafer-Level



High-Aspect Ratio W-filled TSV



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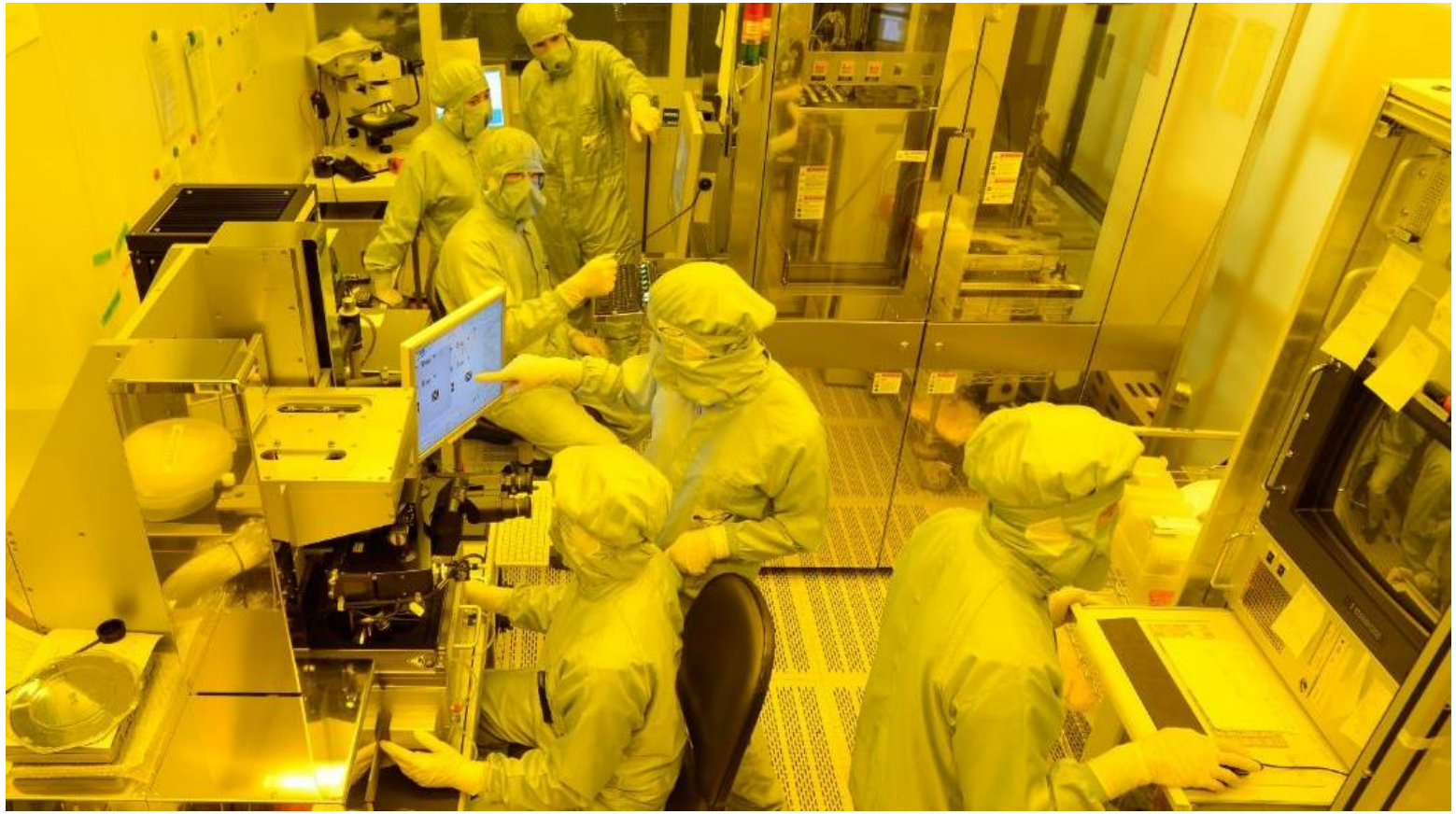
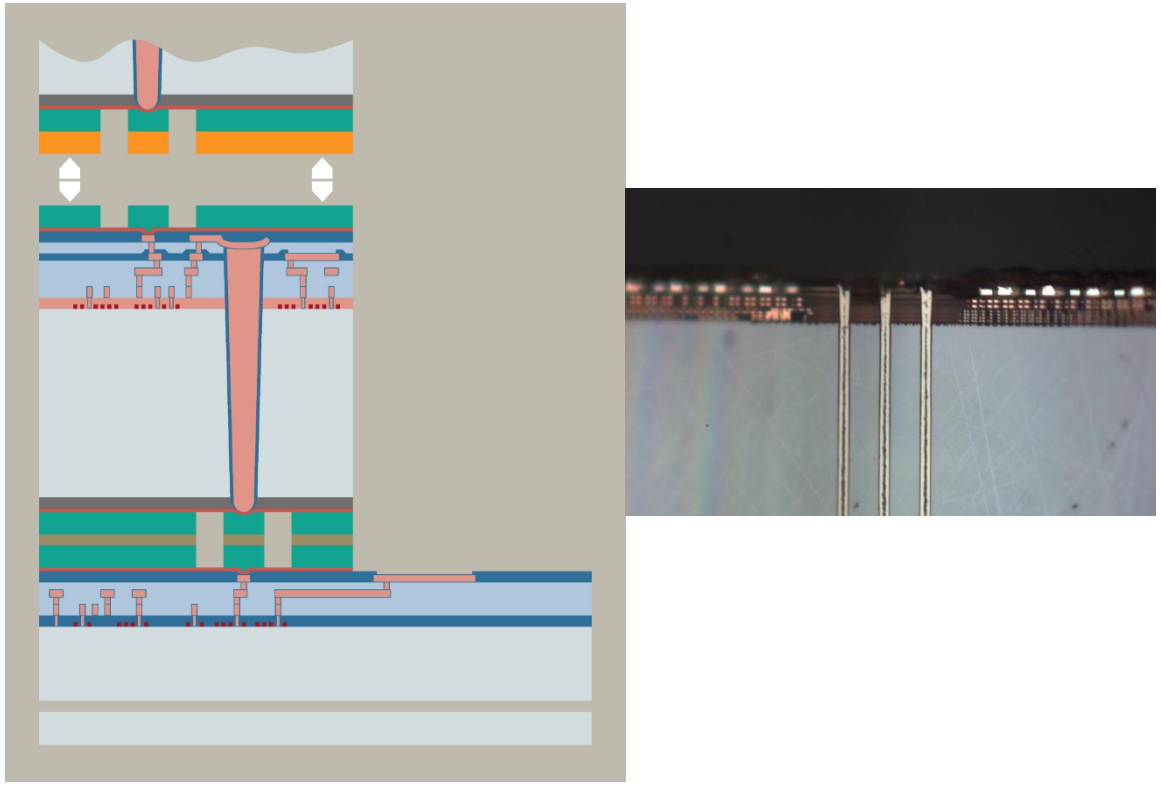
Infrastructure at Fraunhofer EMFT for wafer processing



- Equipment
  - 150mm and 200mm MEMS-Line
  - 200mm CMOS-Line
  - Analytics and test & characterization
  - Backend and thin silicon technologies
- Infrastructure
  - Clean room class 10/100 and grey room (866 m^2)
  - Clean room class 1000 and higher (121 m^2)

EMFTs TSV-SLID technology for 3D-Integration



Key characteristics:

Post BEOL TSV technology

- ❑ Vias before stacking
- ❑ Fabrication of TSVs with standard wafer process sequence

For stacking

- ❑ Simultaneous formation of electrical and mechanical connection
- ❑ Thin SLID layer (~ 10 µm) providing large area metal bond
- ❑ Optimized for chip-to-wafer stacking of known good dies

Source: P. Ramm et al. IMAPS Int. Conf. Device Packaging, Scottsdale, March 9, 2010

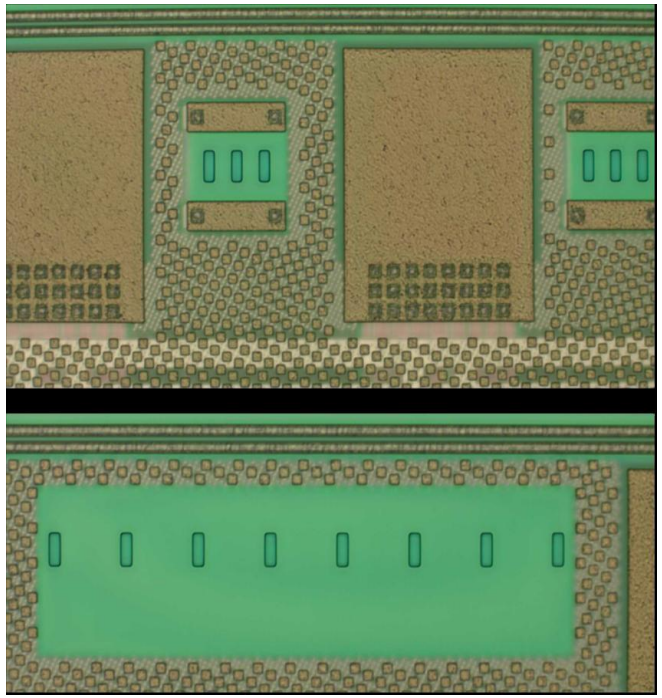
Standard TSV processing at EMFT

Process flow for processing the front-side (ASIC or interposer)

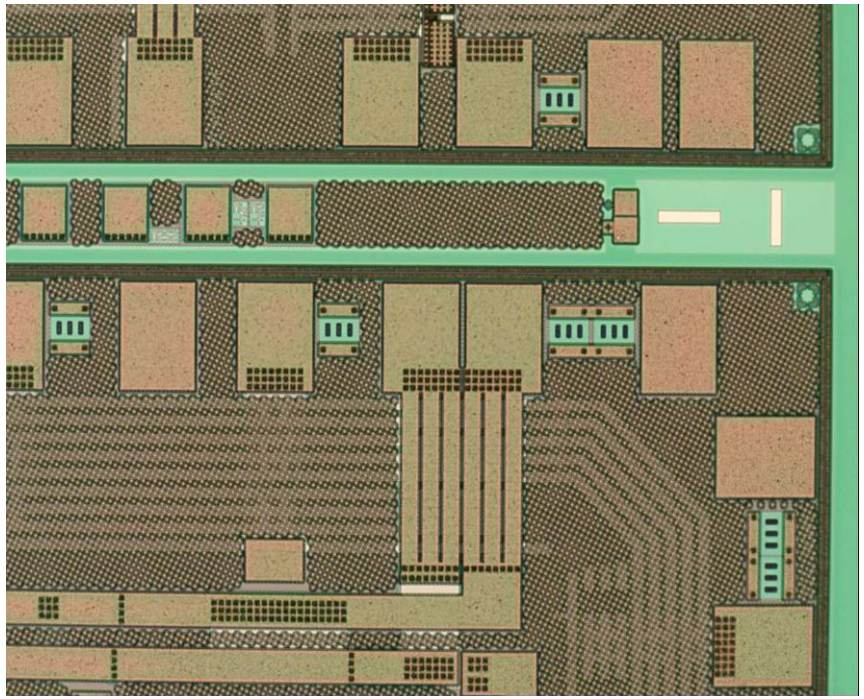
- ❑ Planarisation of ASIC – top surface (if necessary)
- ❑ Hardmask deposition (PlasmaEnhanced-TEOS oxide)
- ❑ Definition of TSV-structures by stepper lithography aligned to ASIC
  (simultaneously definition of alignment marks for backside processing)
- ❑ STS DRIE etching (Bosch process, typical depth 30 µm - 50 µm)
- ❑ Deposition of isolation oxide (SA-CVD TEOS oxide, typ. Thickness 600 nm)
- ❑ Mo - CVD deposition (@ 430 °C) of liner (TiN)
- ❑ CVD deposition ((@ 430 °C) of tungsten (2-3 steps)
- ❑ Etch-Back of W/TiN (maskless and structured)
- ❑ Metal deposition and structuring (AlSi, thickness typ. 800 nm) for wiring of TSV with ASIC-Metal

Design of TSVs (BEOL Approach)

Through-Silicon-Via geometries transferred into eg. ASIC without interfering the physical layout (exclusion areas for metal fill structures have been defined before mask-making).



Micrograph of TSV structures (transferred into resist) adjusted with high accuracy (< 300 nm) to the structures of the ASIC



Micrograph of TSV structures etched (7 µm Inter-Metal-Dielectrics (IMD) and about 50 µm Si-trench) into ASIC-Wafer

DRIE etching with Bosch process

Silicon Deep Reactive Ion Etching (DRIE) for high aspect ratio structures like TSVs

Cycle of deposition (C4F8 plasma cycle for protection depo) and etching (SF6 plasma cycle for etching silicon)

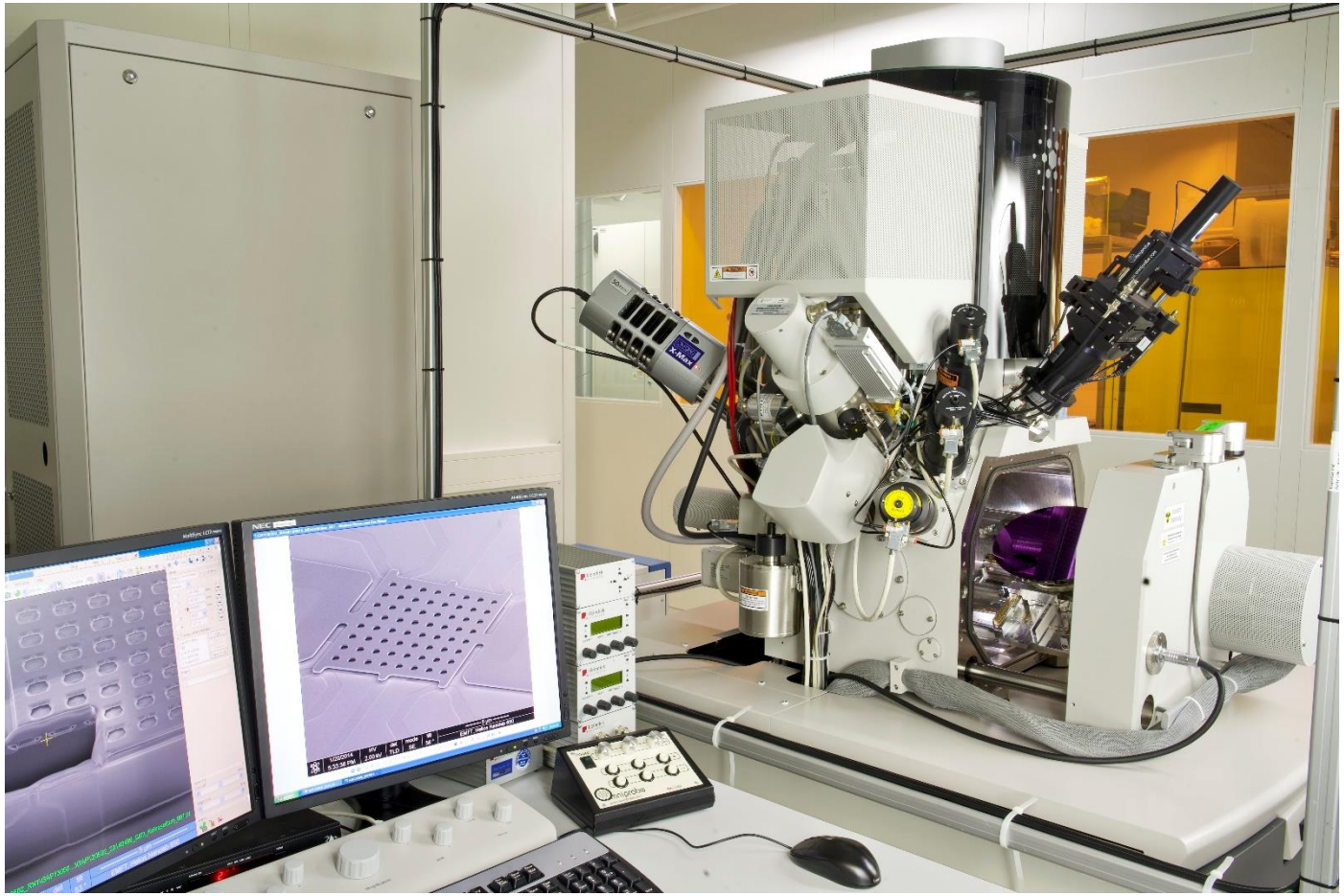
Nearly vertical walls with smooth scallops

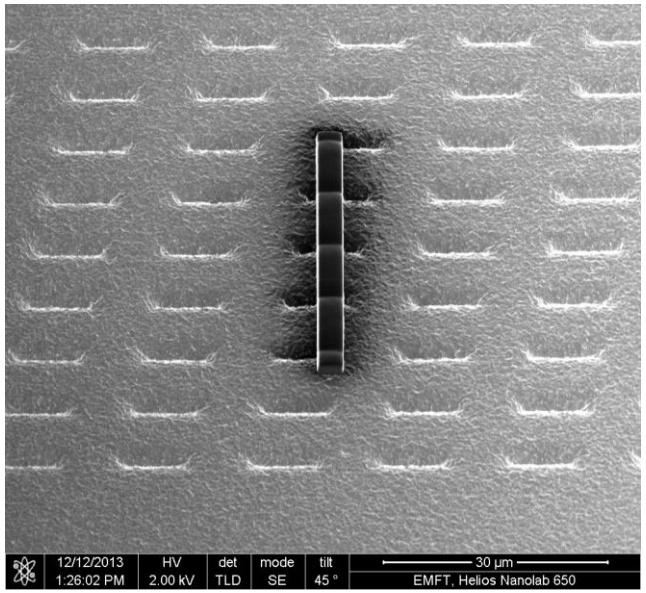
High silicon etch rates can be achieved

Modified and optimised process has been developed

For TSV structuring (typical etch rate for silicon 2 µm/min)

Inspection of TSV processes by using Inline-SEM/FIB





Preparing area of TSV-array for SEM/FIB analysis

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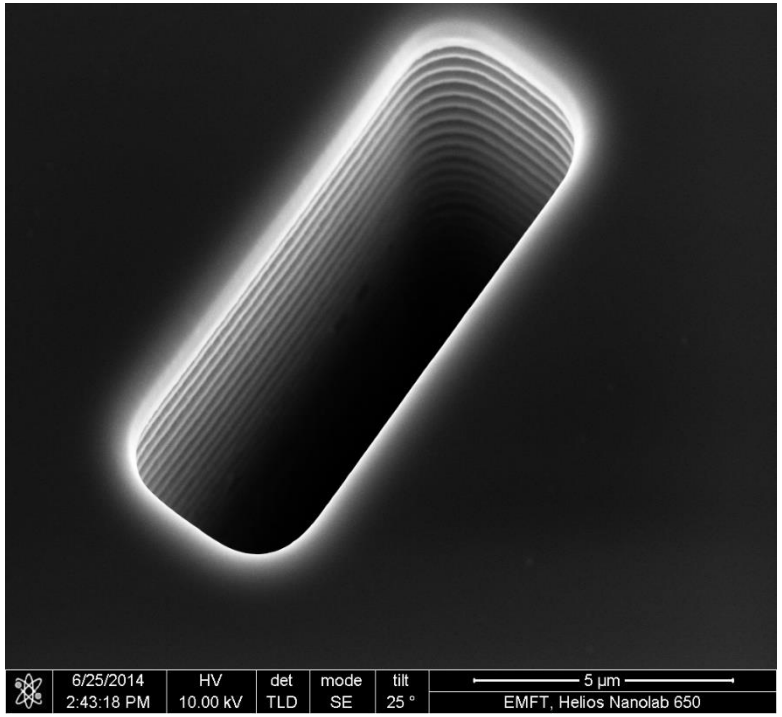
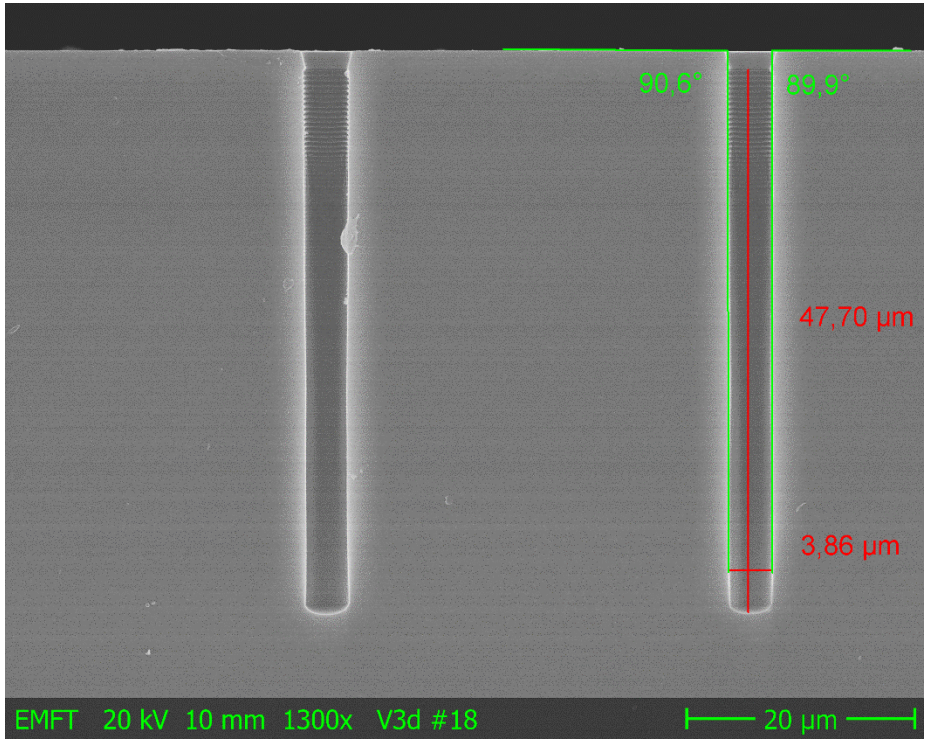
Results after applying DRIE etch processing (Bosch process)



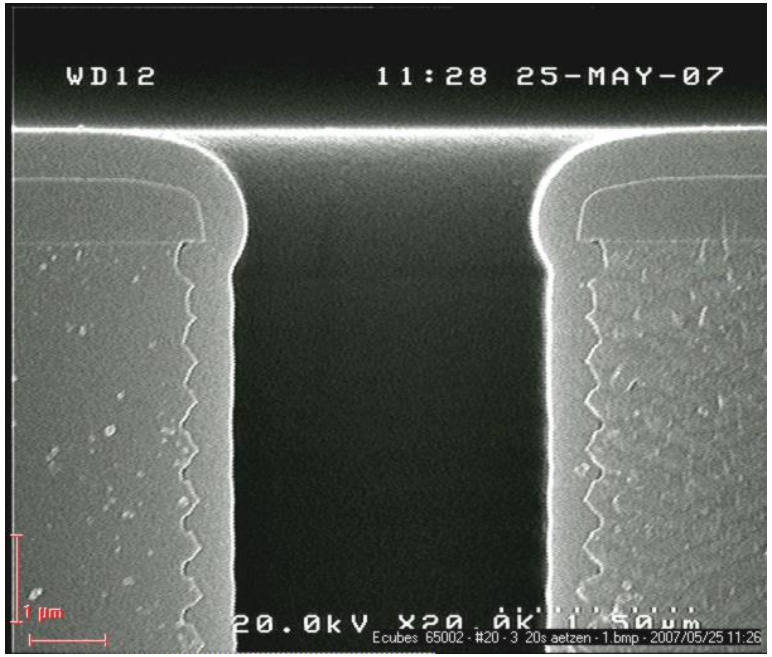
In-line SEM of TSV-structure after applying Bosch process



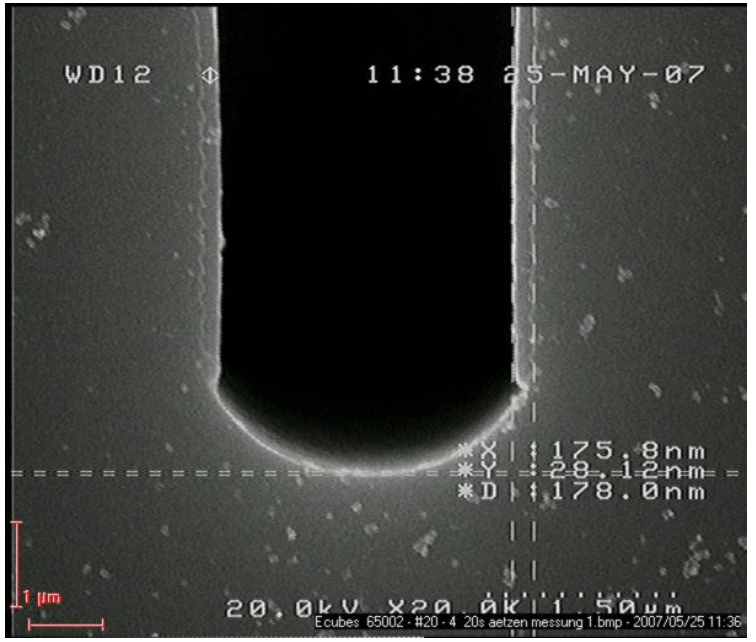
SEM shows nearly 90° taper angle

(etch depth apporx.50 µm, AR > 12:1

Results after depositing SA-CVD oxide (isolation oxide)



SEM shows smoothing of scallops



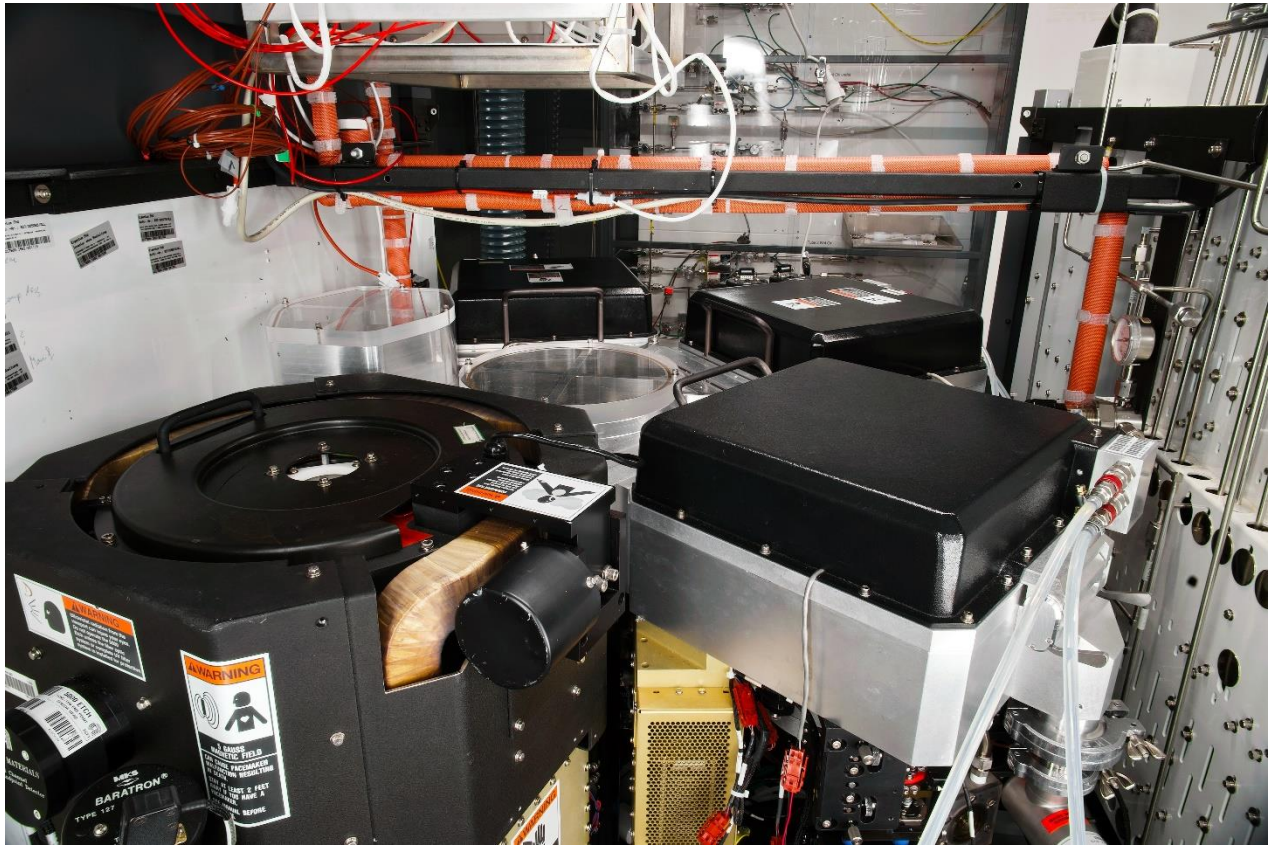
Conformity of desposition approx. 45 %

Source: A.Klumpp, R. Wieland, Fraunhofer EMFT

IEEE-International Workshop on 3D System Integration

Munich,October 1-2, 2007

Equipment for TiN/W processing



Multi-chamber (200 mm wafer)

P 5000 System of AMAT

Process gases

TDMAT
(Tetrakis(dimethylamido)titanium)

precursor for TiN deposition

WF6 for W-CVD deposition

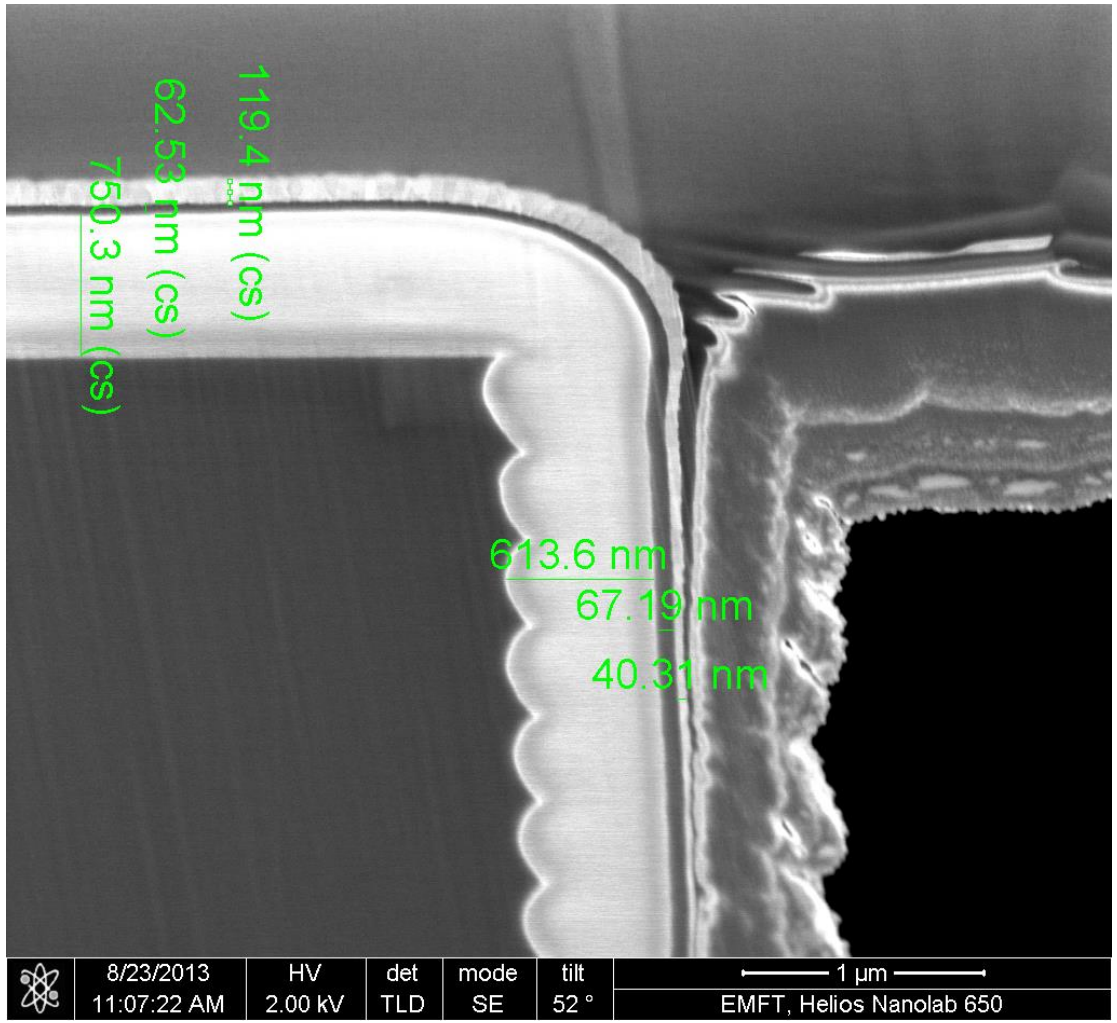
Results after depositing TiN –layer and testing W-seed

SEM shows

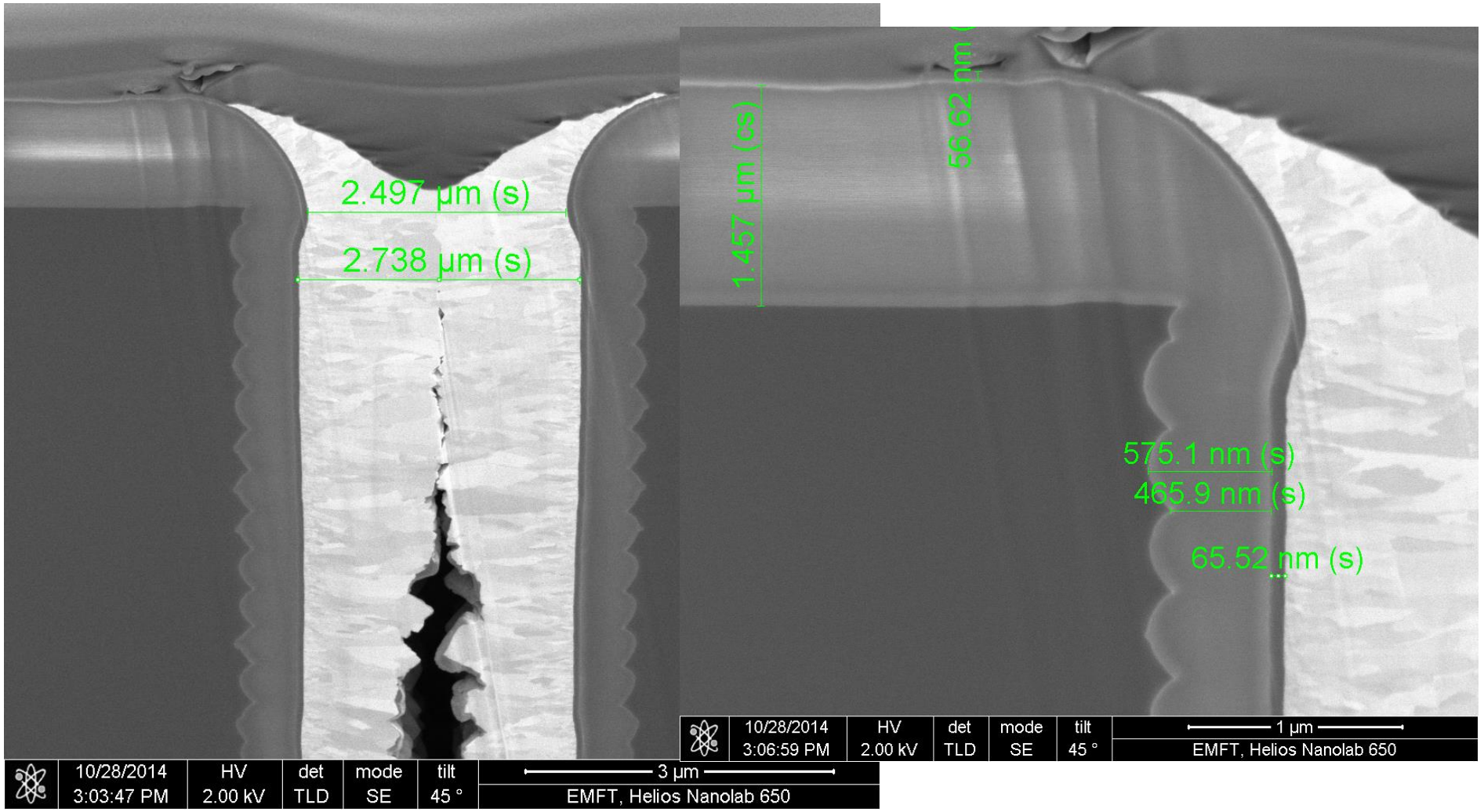
smoothing of scallops

Conformal TiN-layer deposition

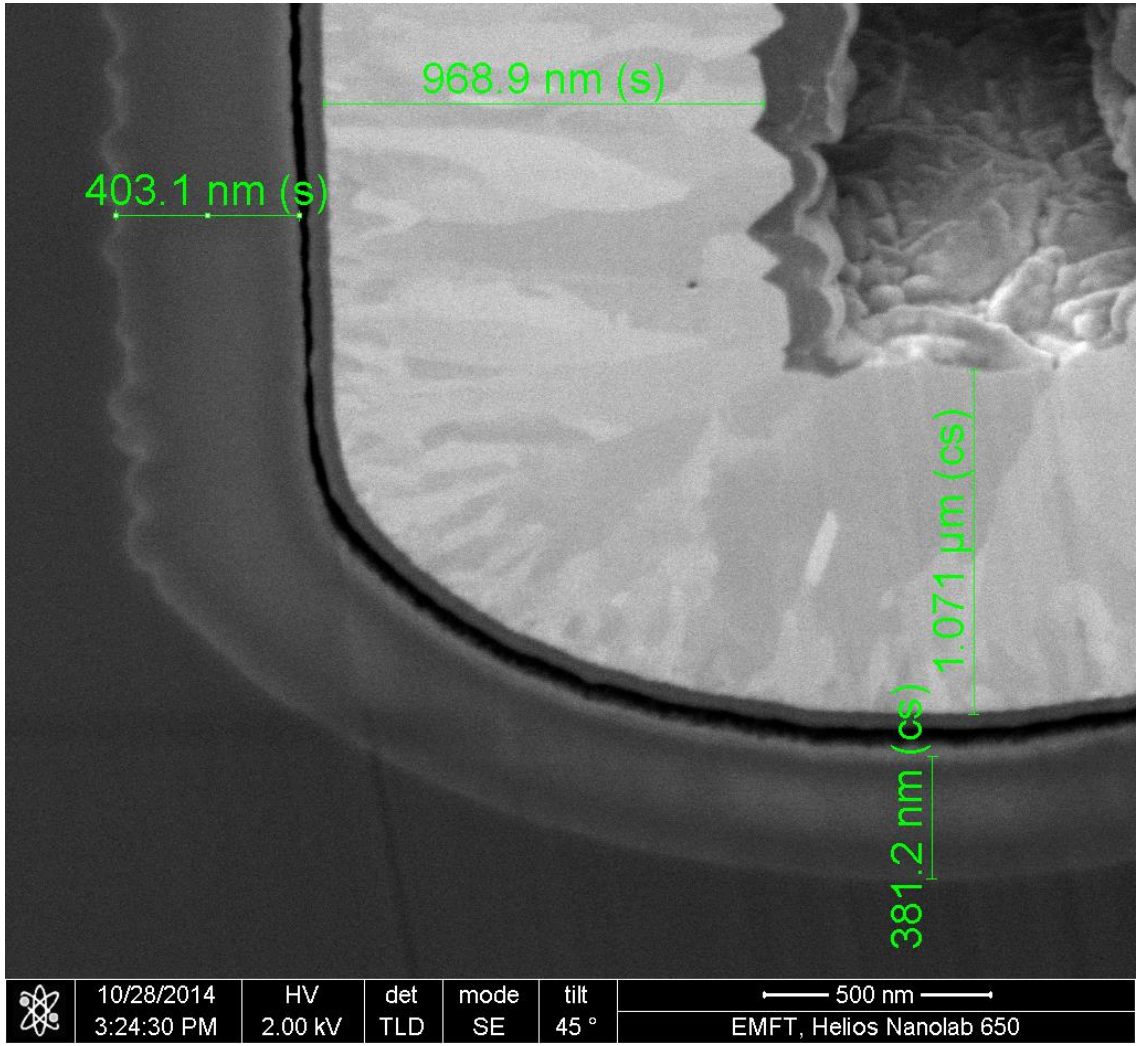
Deposition of W-seed



SEM of W-filled TSV at top of the trench



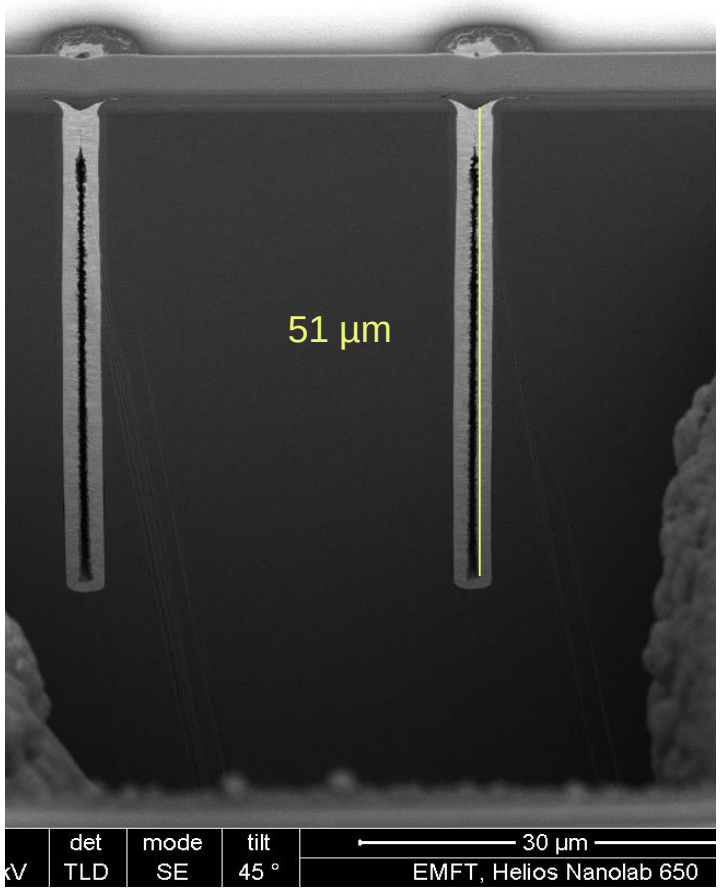
SEM of W-filled TSV at bottom of the trench



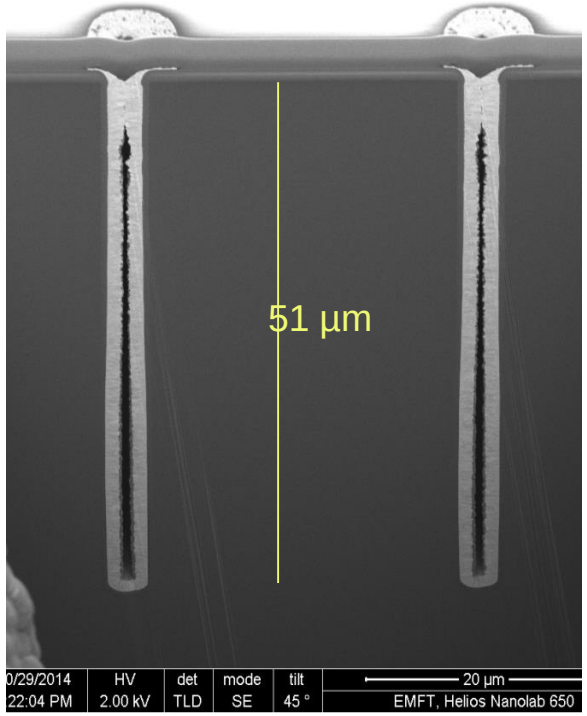
W-filled TSV technology at EMFT

SEM pictures after etch-back of W/TiN show homogeneous processing

center of the 200 mm wafer



near notch of the wafer



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W- Filled ultra-compact TSV-array

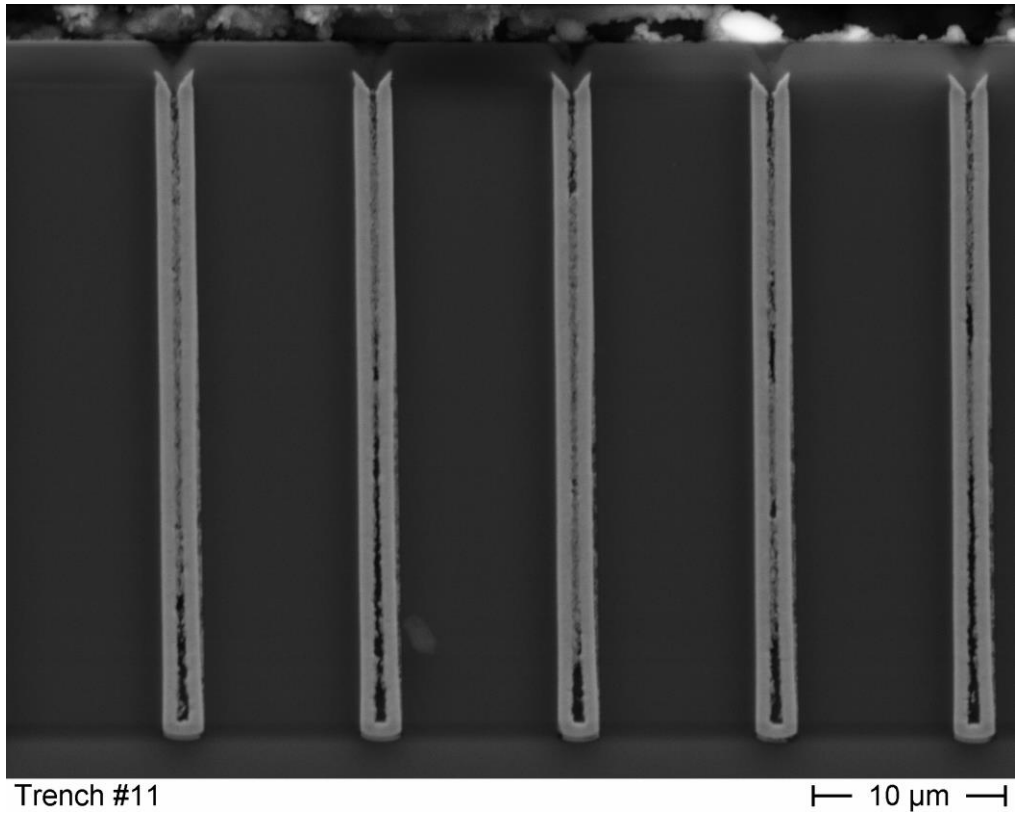
TSV –Dimensions

3 µm x 10 µm x 50 µm

300 nm SACVD TEOS

20 nm TiN CVD

900 nm W CVD und W Backetch

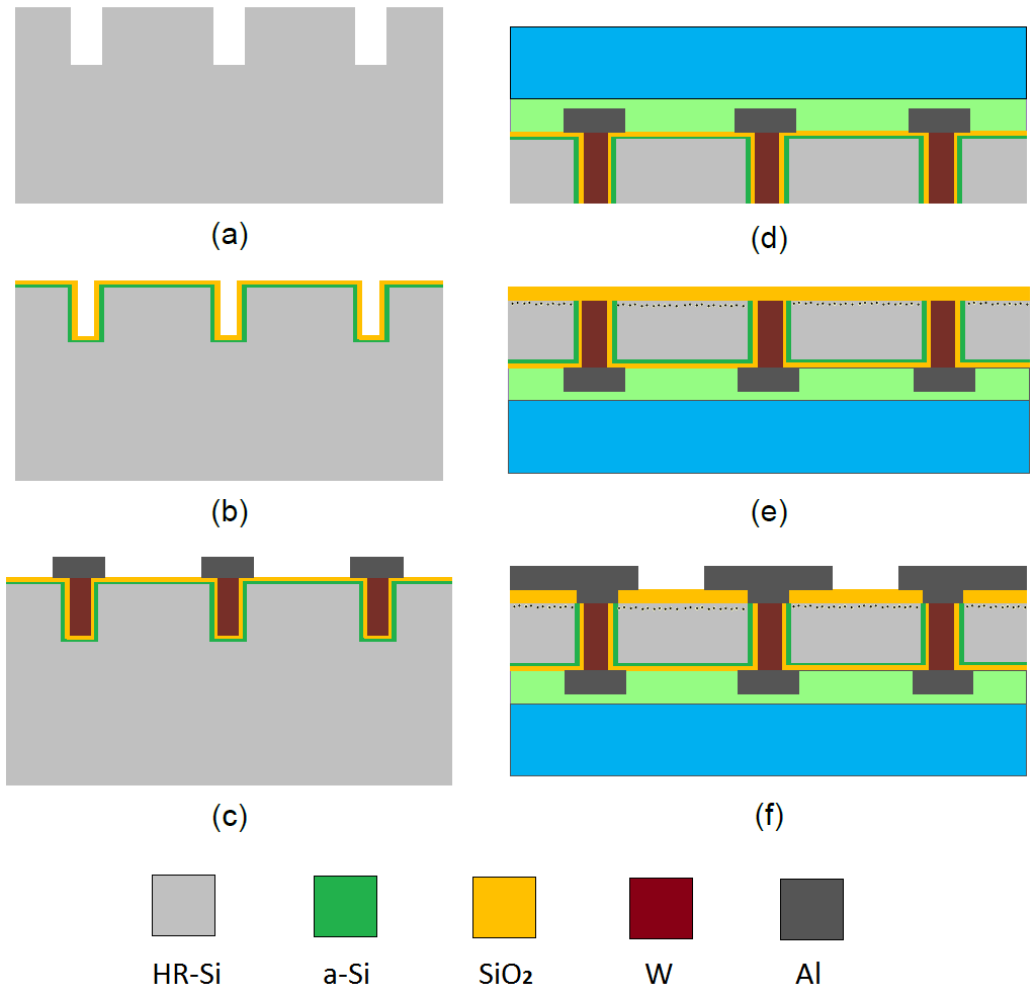


Source: A.Klumpp, R. Wieland, Fraunhofer EMFT

IEEE-International Workshop on 3D System Integration

Munich,October 1-2, 2007

Back-side processing of RF modules



Gluing of Handle substrate

(Polymer on both wafers)

Grinding, stress relief etch,

short Si-CMP

STS etching for uncovering the TSV's (incl. stepper alignment marks)

Oxide deposition (low temperature 130 °C)

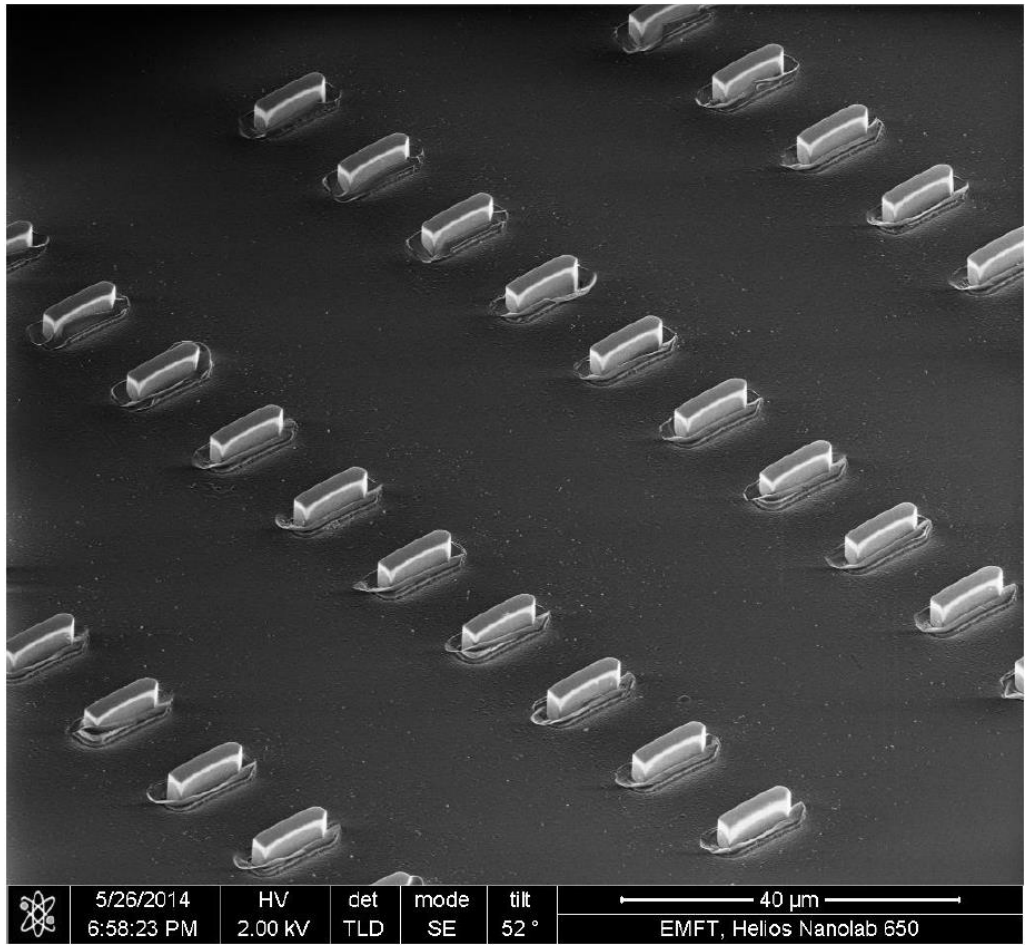
Oxide CMP

Oxide Dry etch

Metal deposition (low temperature)

Metal structuring (low temperature)

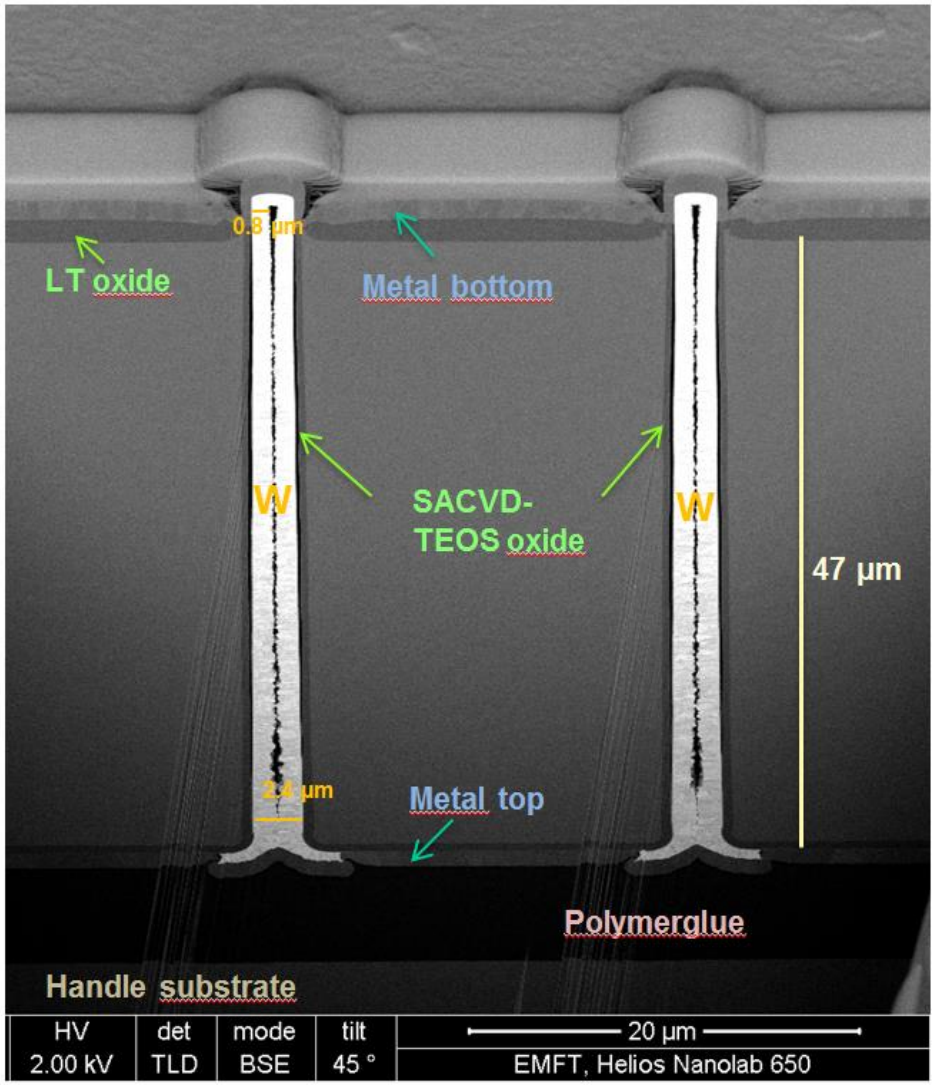
SEM top view of TSV‘s on the back-side after oxide etching



Array of W-filled TSV‘s prepared for wiring from the back-side

Finished processing of W-filled TSV

SEM cross view of FIB-prepared TSV's after deposition of back-side metal



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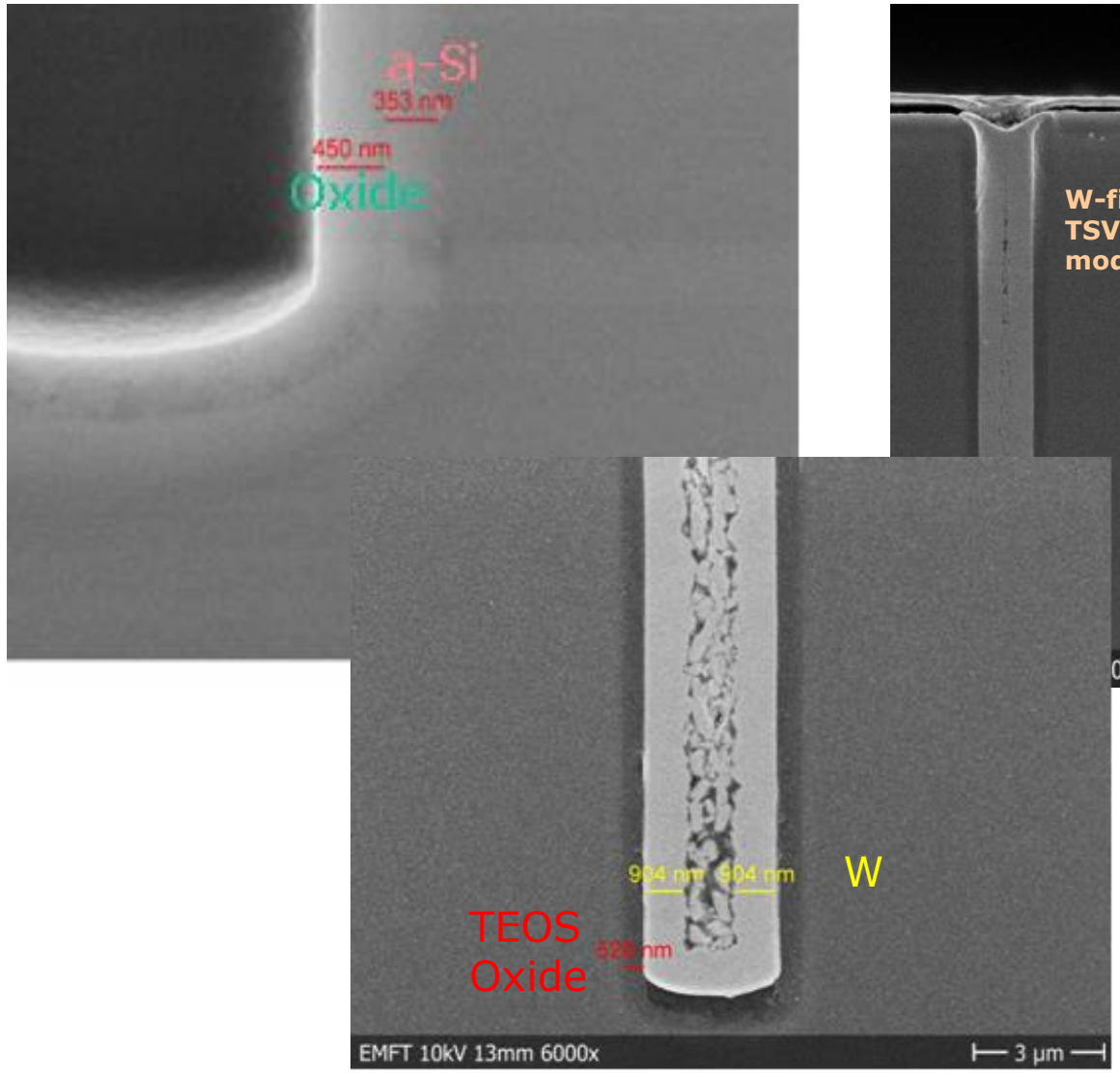
Development of 3D-Integration by W filled TSVs for RF requirements

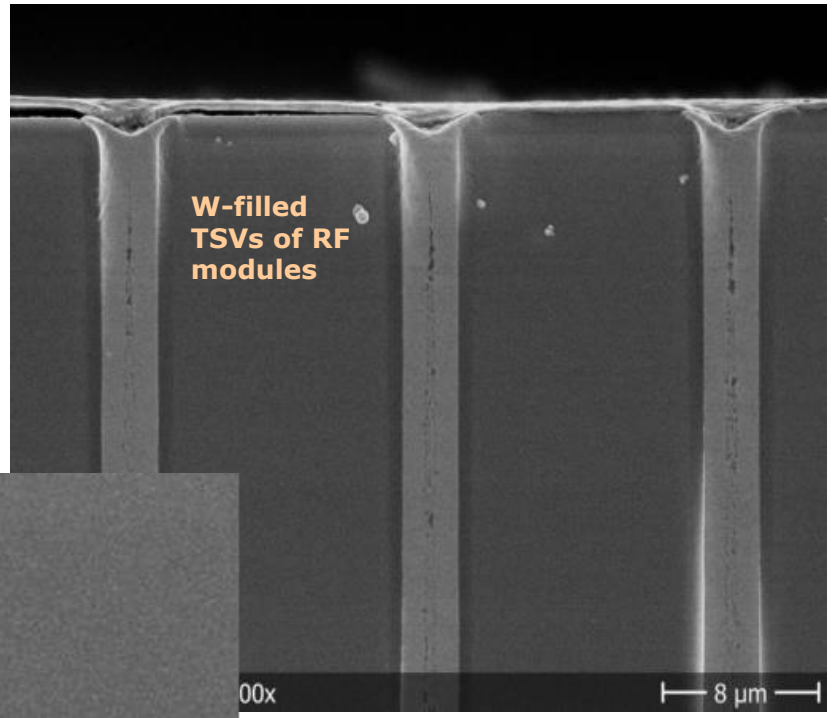
Choose of high-ohmic silicon substrate (4.5 kOhmcm)

Modifications to the standard Process flow for processing the RF modules

- ❑ Definition of TSV's (enhancing lateral dimensions of TSVs)
- ❑ Removal (BOE wet etching) of all oxide after TSV etching
- ❑ Deposition of an amorphous silicon layer (typical 500 nm) by LPCVD process (@ 560°C)
- ❑ Enhancing the thickness of the metal (AlSi) –wiring to approx. 1.5 µm

SEM of W-filled TSVs for RF-Application





J. Weber,

3D-IC Conference 2016

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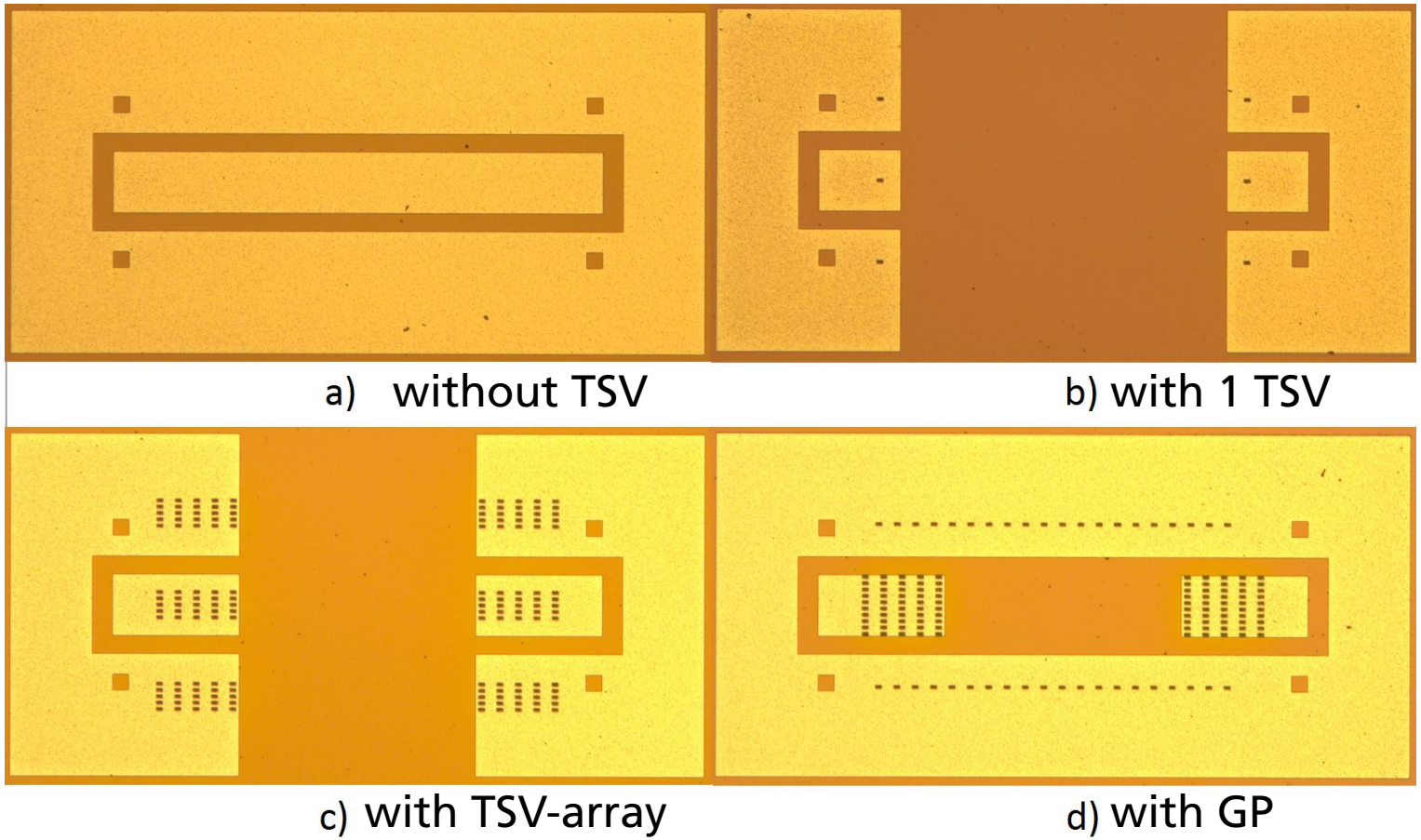
Application example Standard Coplanar Wave Guides (CPWs) with and without TSVs and ground planes



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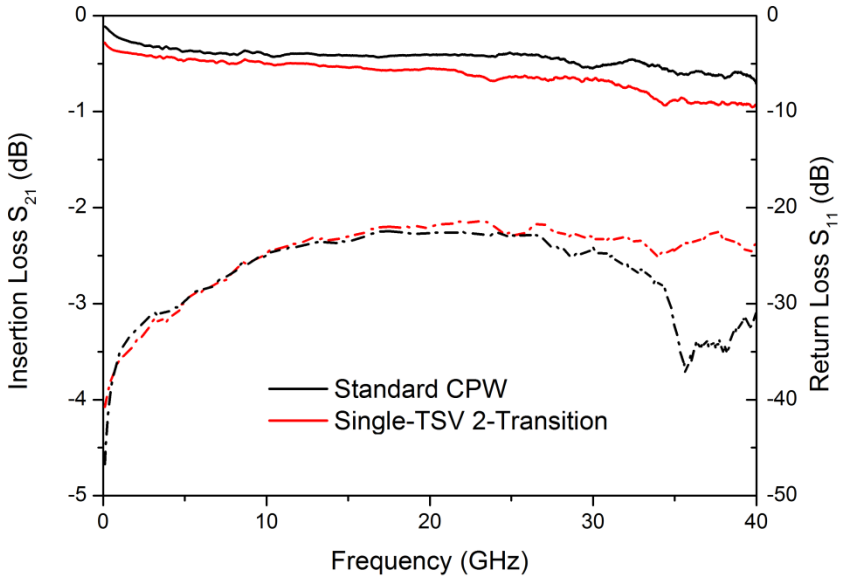
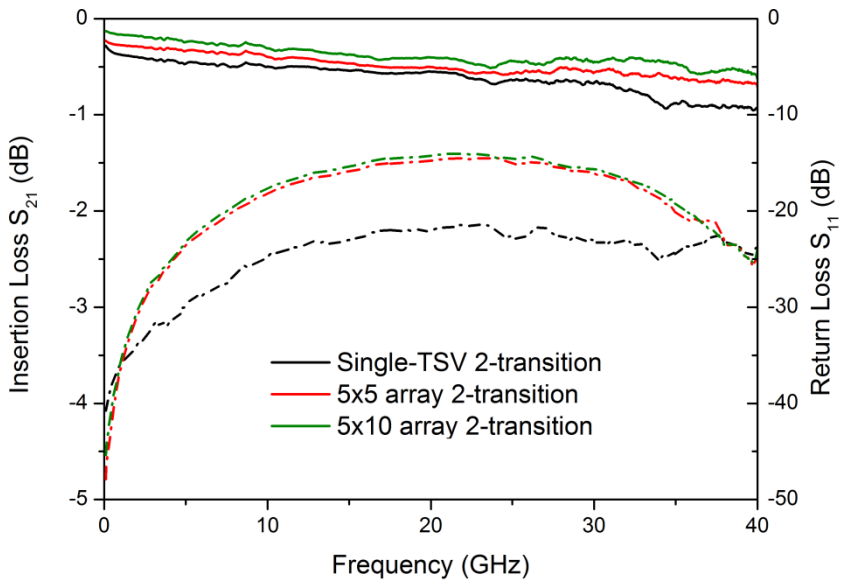
Measurement of S parameter of CPW (1mm)

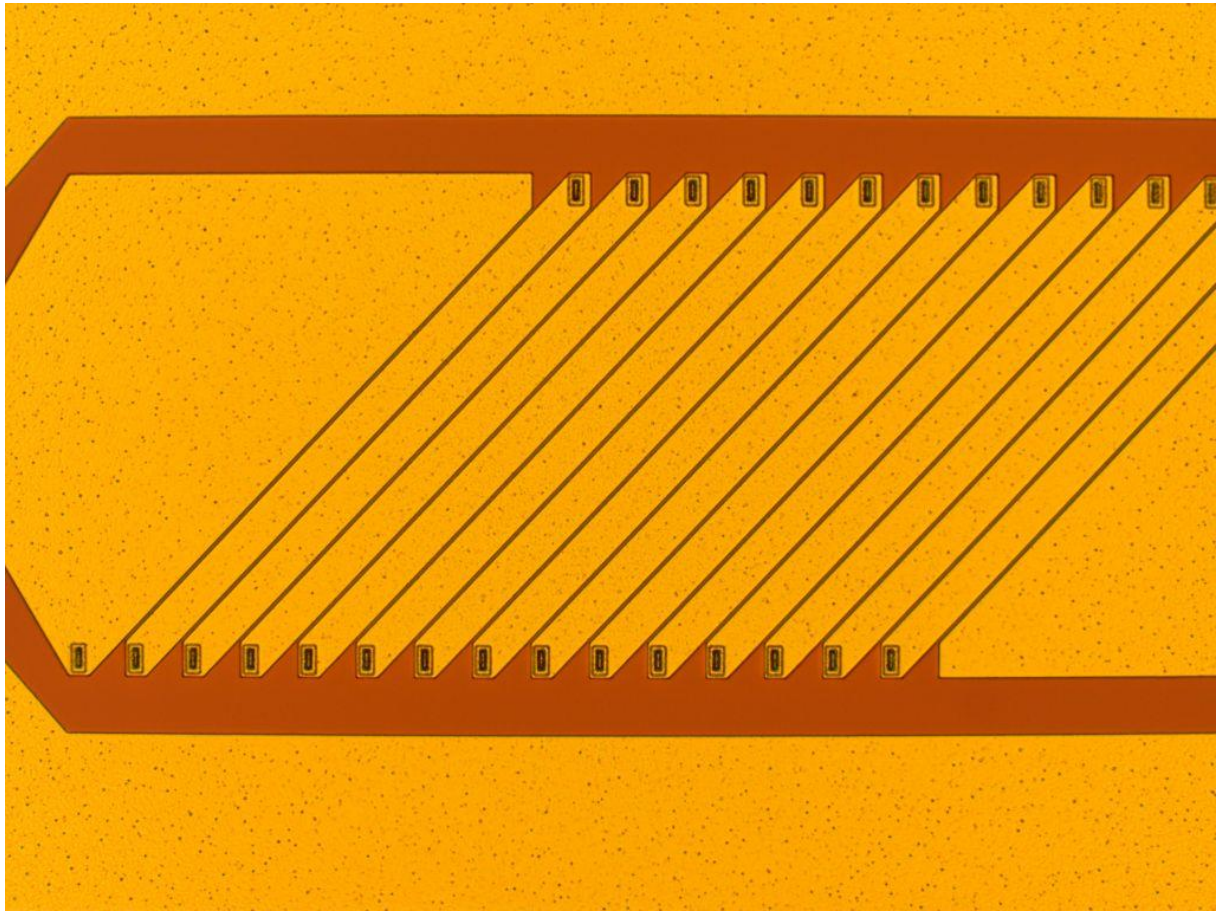
(Source: W. Vitale at EPFL)





Fine-pitch TSV-technology allows arrays of e.g. 5x5 TSVs which reduce the insertion loss at 10 GHz down to 0.014 dB per transition.

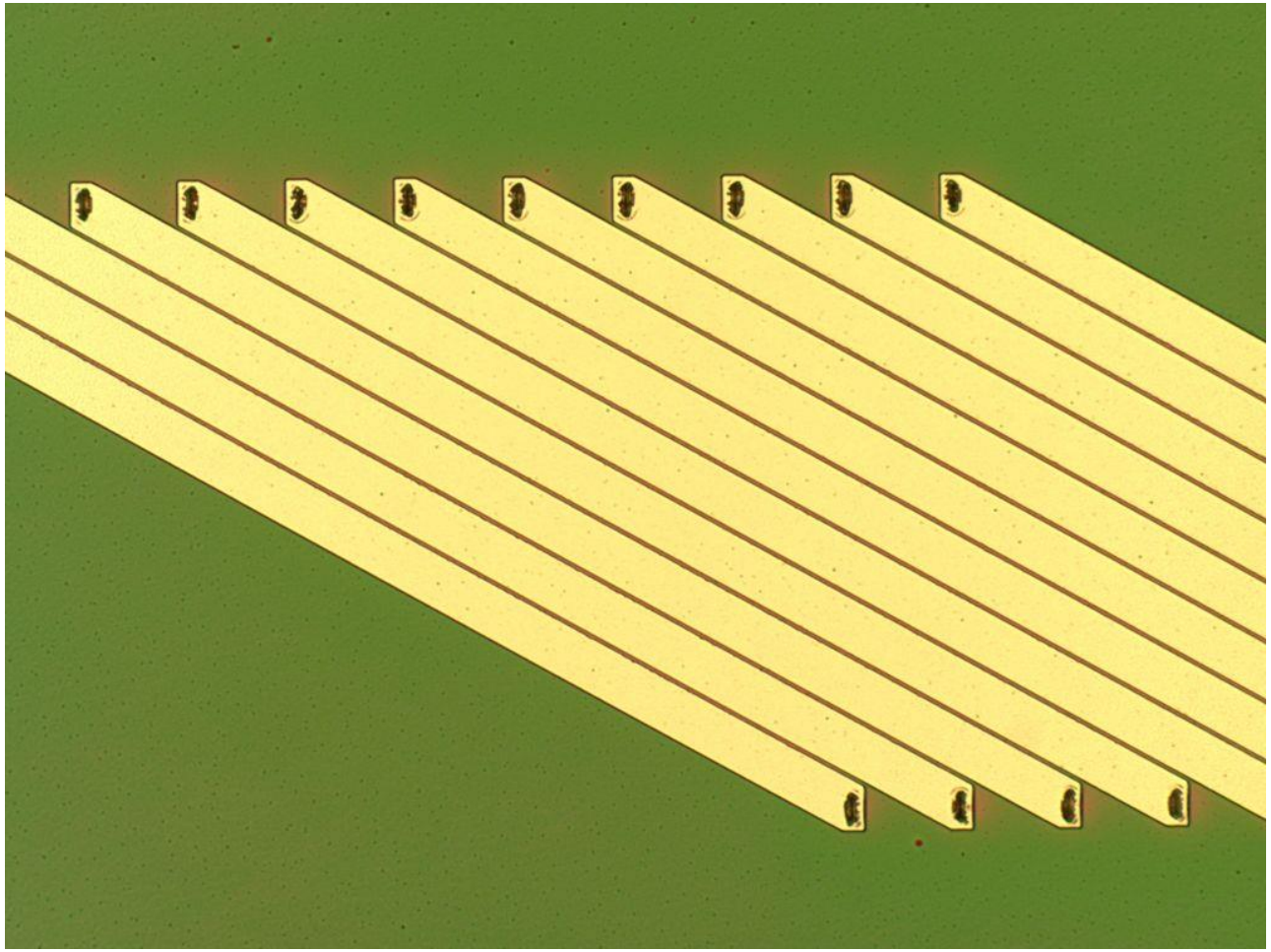
Application Example: 3D TSV integrated ultracompact inductor



Top-view of inductor structure (front side) after W-deposition and W- and metal structuring

Design and measurements:
W. Vitale, EPFL Switzerland

Application Example: 3D TSV integrated ultracompact inductor

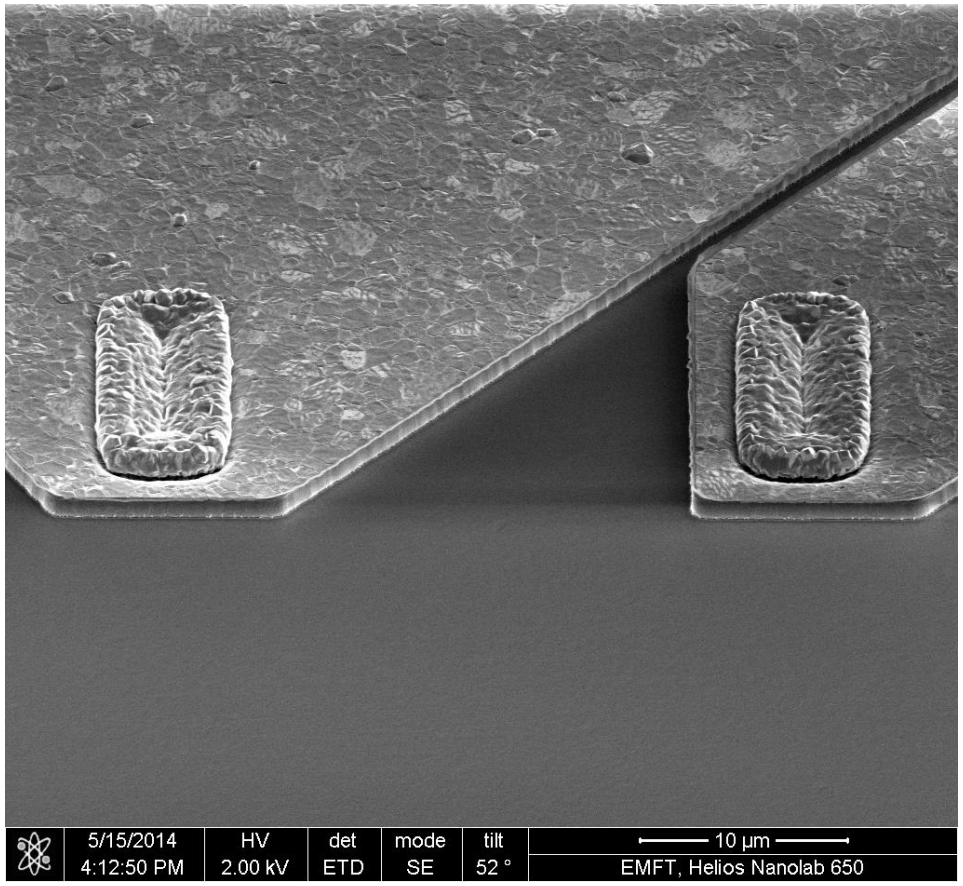


Micrograph (top-view) of backside metallisation

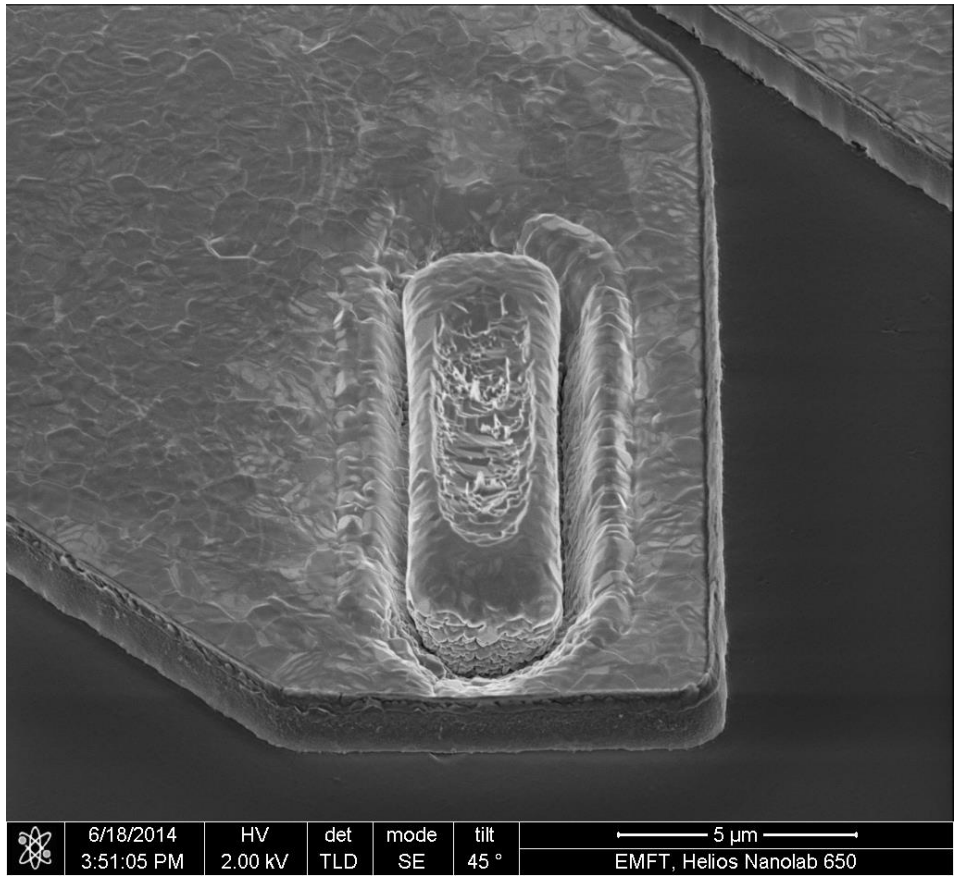
3D TSV integrated inductor after metal structuring

SEM top-view on metal-structure connected with W-TSV

frontside



backside



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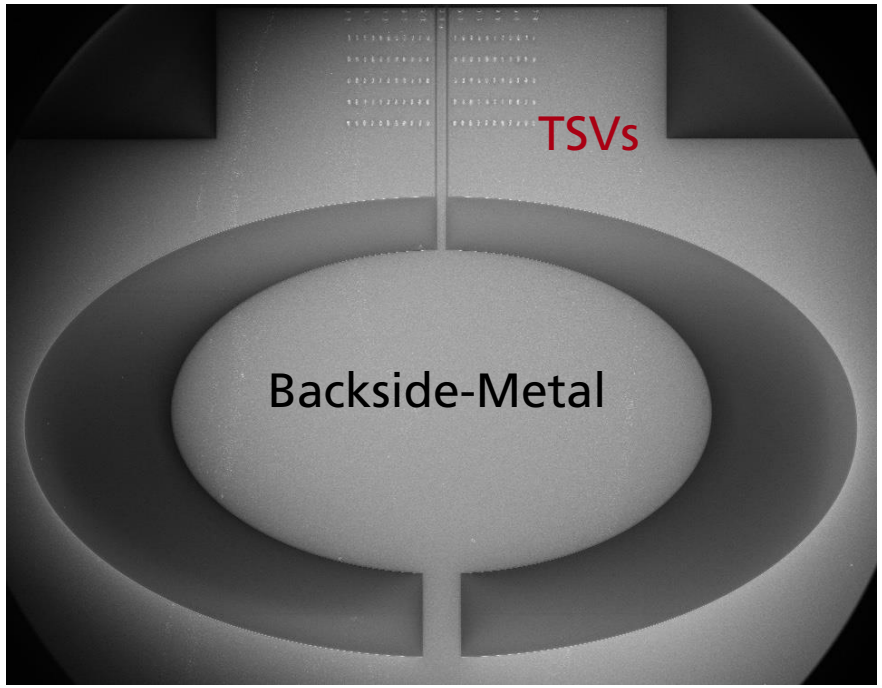
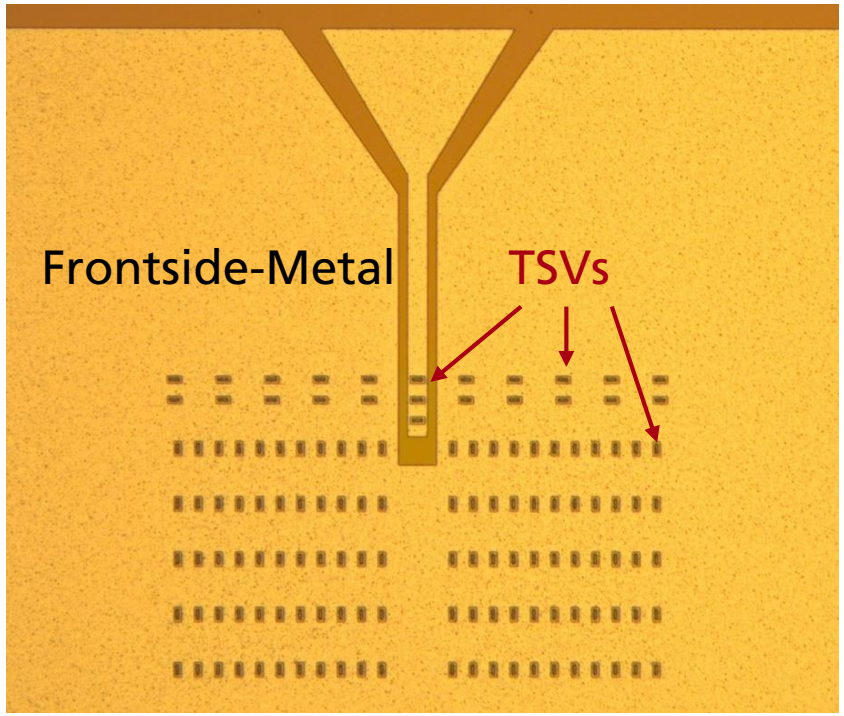
Application: 3D-TSV integration of mm-wave antenna (60 GHz)

Radiation part of the antenna on back-side of chip



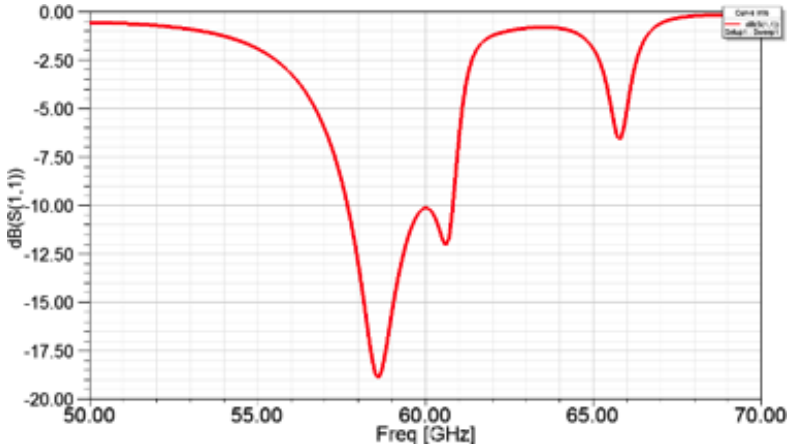
CPW feeding line placed on top of the chip



Design done at IMEC Institute (W. deRaedt)

MM-wave antenna simulation and measurement
(done at KU Leuven/IMEC by W. deReadt)

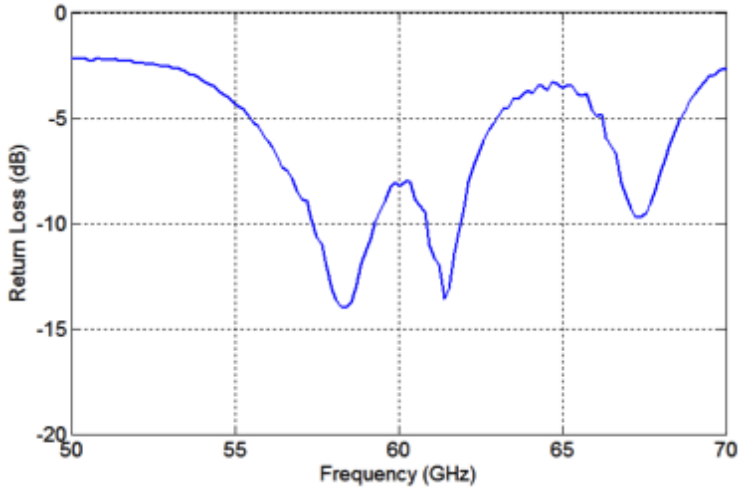
Simulated Return loss (50 – 70 GHz)
(ANSYS/HFSS)



Measured return loss (50 – 70 GHz)

Optimizing of loss by implementation of de-embedding structures possible

Special set-up shows that the input impedance is very close to the value when it would be measured in true free space conditions.



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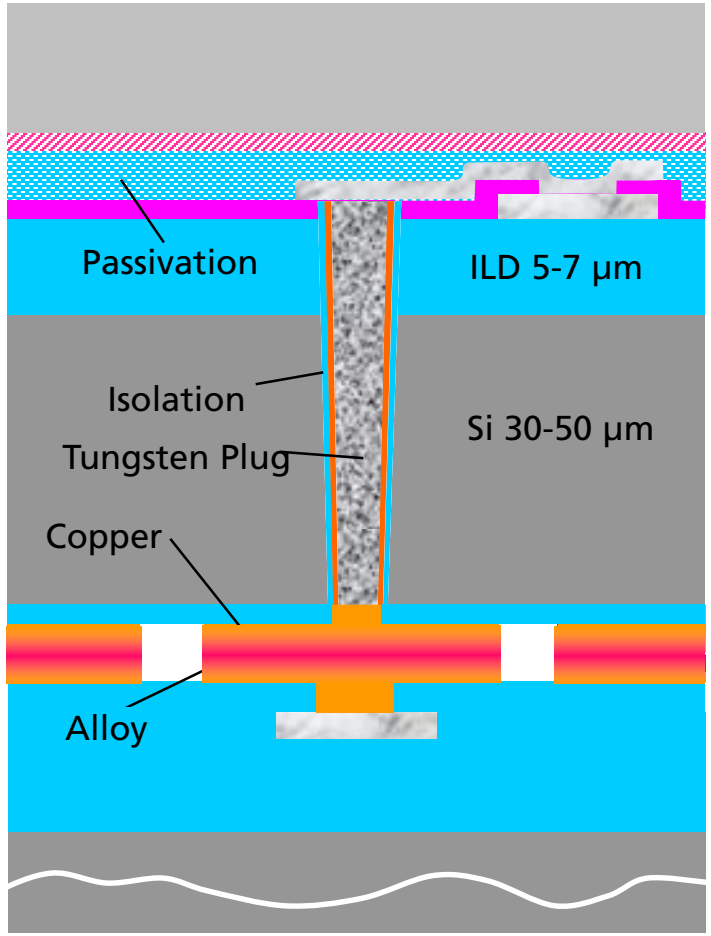
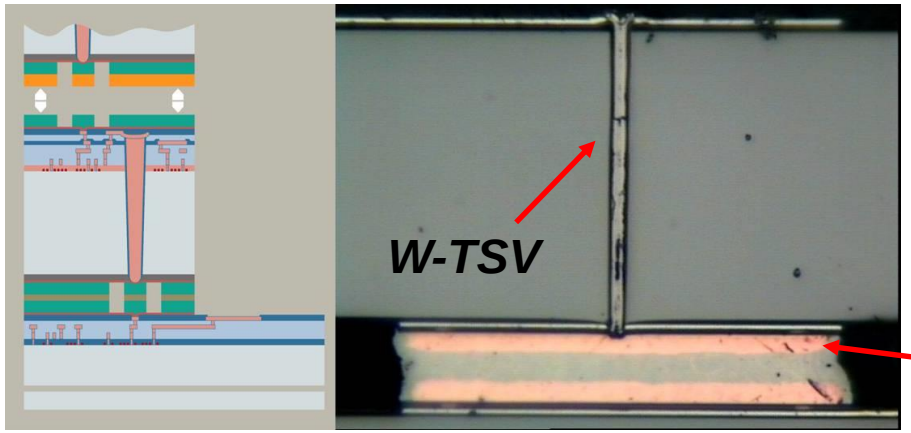
W-TSV technology combined with SLID-technology for Waferbonding



- Fabrication of Tungsten-filled TSVs on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of TSVs (backside)
- Backside metallisatin
- Definition of SLID-Pads
- Through Mask Electroplating
- Chip/Wafer Alignment and Soldering

SLID (Solid-Liquid_InterDiffusion in this case for Cu/Sn-System)

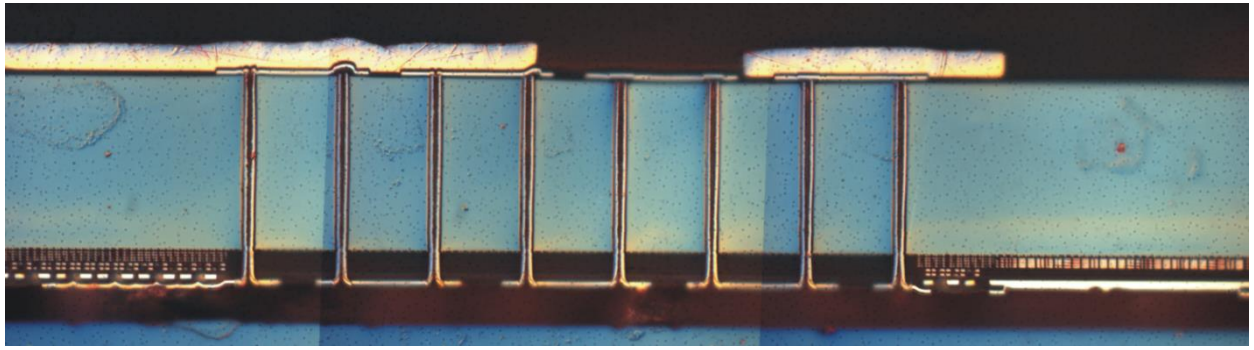
3D-Integration an der Fraunhofer EMFT: TSV-SLID

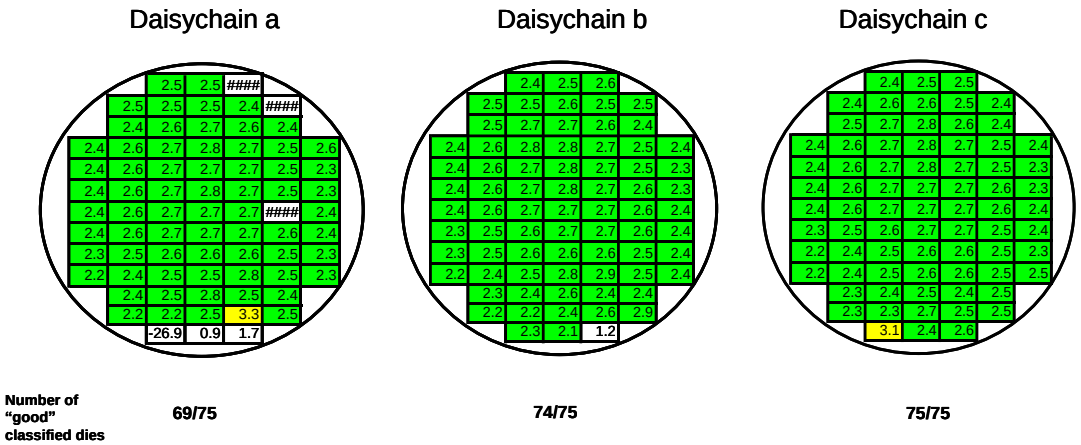


Post BEOL 3D-Integration

Cu-Sn SLID (Solid Liquid Interdiffusion)

Process control module (PCM) for TSV-technology





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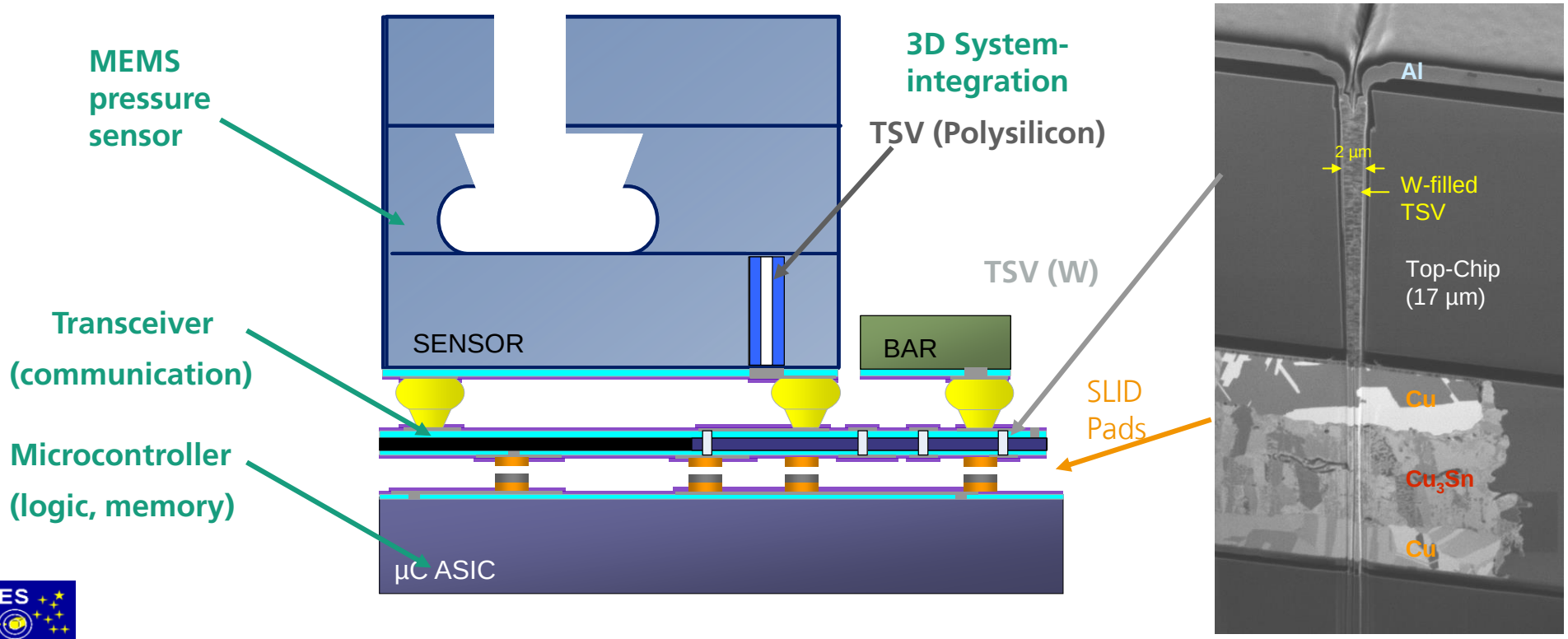
Application for Heterogeneous System Integration with W-TSVs

Infineon´s Tyre Pressure Monitoring System – TPMS



e-CUBES

EU Project with Infineon, SINTEF and EMFT

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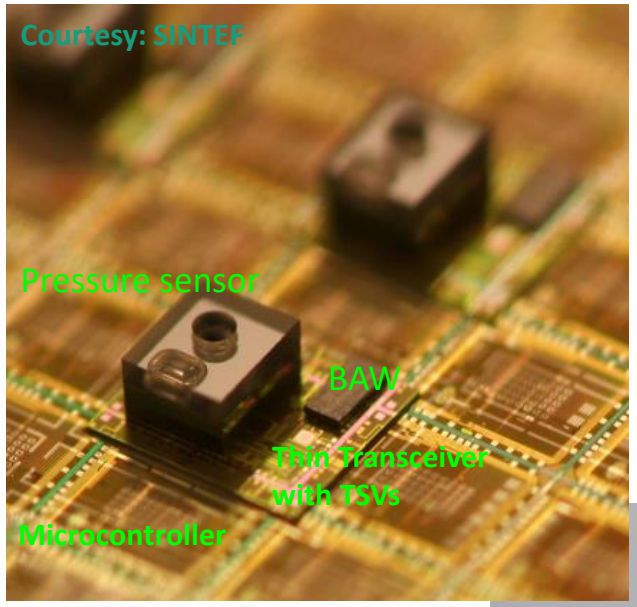
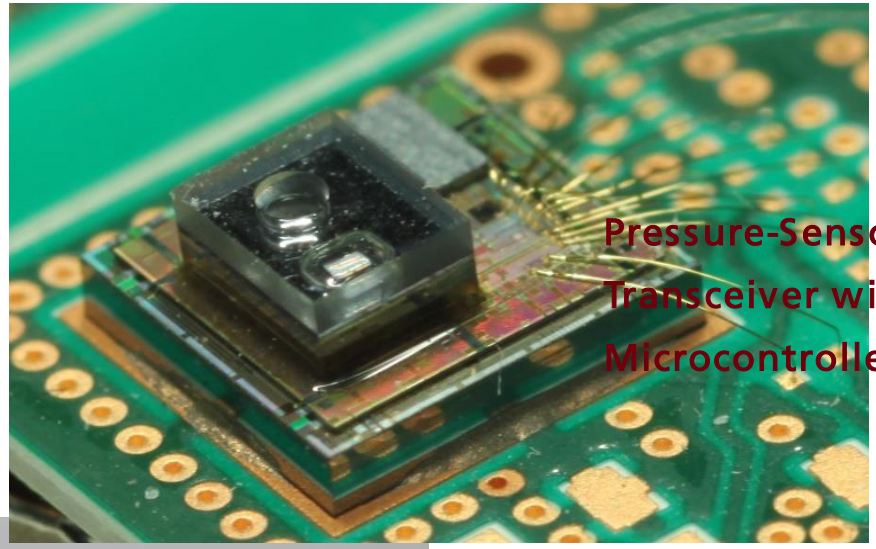
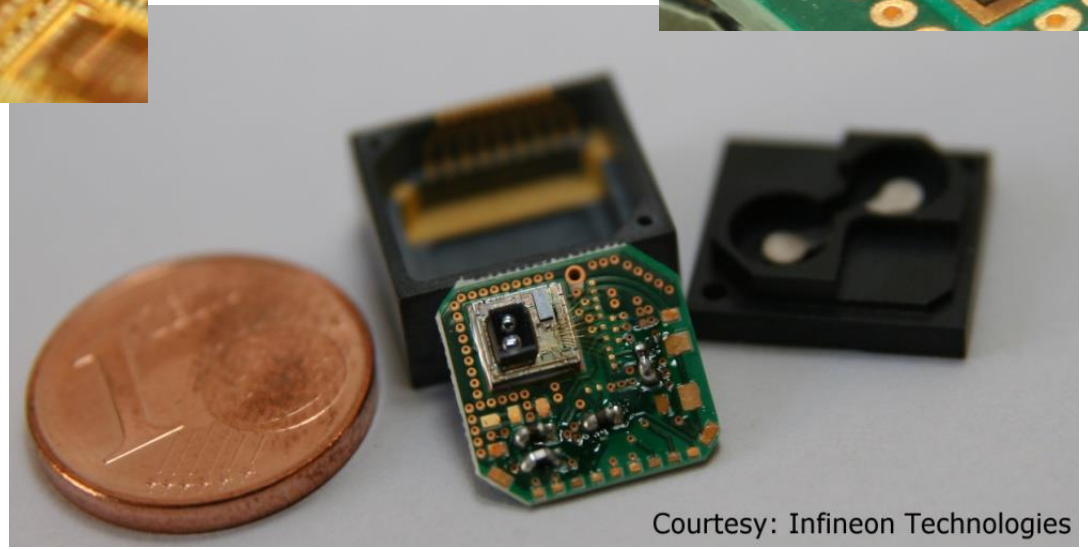
3D TSV integrated MEMS/IC stack for TPMS





Automotive Demonstrator of Infineon within European e-CUBES project



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Main Features of Fraunhofer EMFTs TSV-SLID Technology

- Post Backend-of-Line (BEOL) technology (use of fully fabricated wafer)
- Wafer scale process
- Wafer-to-wafer stacking or chip-to-wafer stacking (KGD)
- Typical dimensions:
  - TSV lateral dimension in silicon: 3.9 x 10.9 μm^2
  - Min pitch TSVs: 10 µm
  - SLID pads: 30 x 30 μm^2, min pitch 60 µm (standard)
    5 x 5 μm^2, min pitch 10 µm (high resolution)
  - Interconnect density: 10^3-10^4 mm^{-2}
  - Stand-off height SLID layers: ~10 µm
- Typical resistivity per interconnect

  250 mOhm (tungsten, 3.9 µm x 10.9 µm x 50 µm) incl. SLID
- Reliability

  based on simulation results: Regions of high stress and strain: the via itself (in case of Cu TSV), upper and lower end where the BEOL metal layers are connected (in case of W TSV)

Conclusion

- Fraunhofer EMFT offers very flexible 3D-integration technologies
  - W-TSV combined with SLID (for BEOL processing of processed wafers)
  - Low temperature SLID (die to wafer)
  - Low temparutere oxide-bond
- Broad range of applications
  - MEMS/IC Integration -> IoT
  - Detector / read-out circuit
  - Analog / CMOS device integration
- Typical Project partners
  - Semiconductor industry and R&D institutes within funded projects (e.g. European Commission projects)
  - MEMS supplier, R&D organisations and institutes

Acknowledgement

Main co-working colleagues of Fraunhofer EMFT:

Robert Wieland (Head of CMOS): Development of Bosch process and W-CVD for HAR TSVs

Armin Klumpp (New topics): Project management within 3D-Integration

Reinhard Merkel (Sensor & Mirosystemintegration):
Assembly, thinning and Waferbonding

Lars Nebrich (Business development)
Design, Layout and process flows

Martin Heigl ((Sensor & Mirosystemintegration):
Metrology In-line FIB/SEM

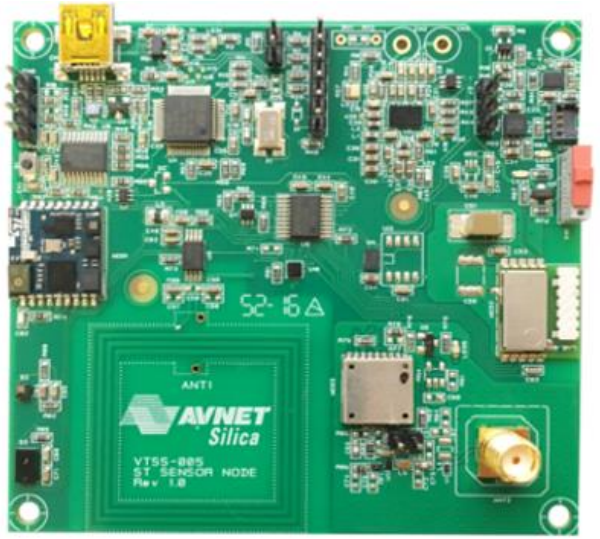
Ulrich Schaber (CMOS group): TiN/W-CVD processing

Peter Ramm (Strategic projects): Pioneer of 3D-Integration at Fraunhofer EMFT

Outlook for Application example

Heterogeneous 3D-TSV Integration of Sensor Nodes

Classic IoT-Sensornode

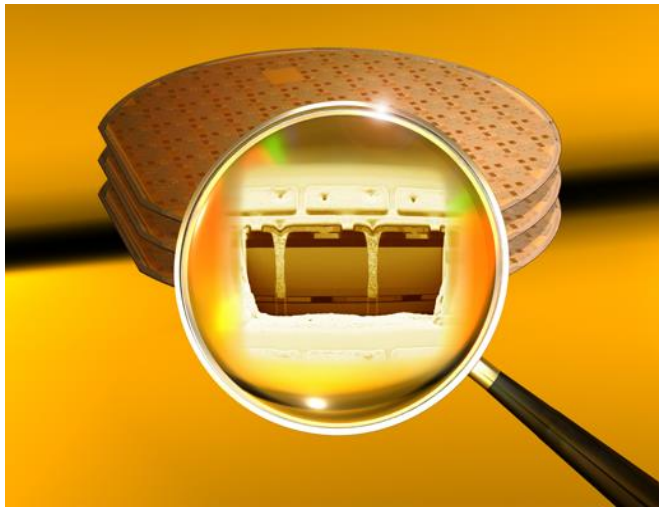


PCB of IoT-Sensor-node

Source:

MEDIZIN elektronik
powered by elektroniknet

3D-Heterogeneous Integration



Source:

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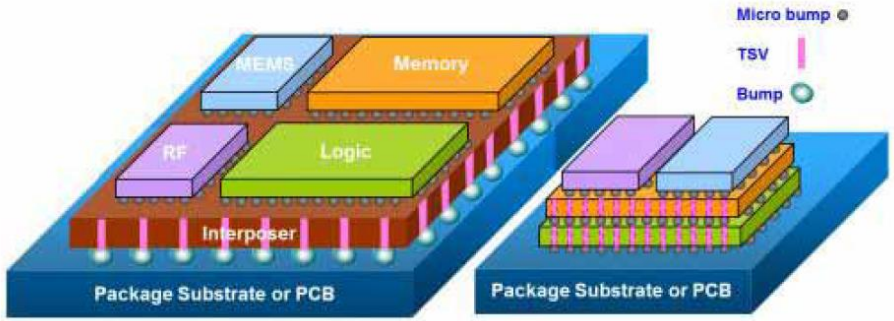
2.5D/3D-heterogeneous integrated Sensorsystem



Source:

Yole: http://www.i-micronews.com/lectureArticle.asp?id=8836

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Thank You For Your Attention !

Fraunhofer EMFT
Hansastraße 27d
80686 München
Tel. +49 89 54759 - 539
josef.weber@emft.fraunhofer.de
www.emft.fraunhofer.de

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