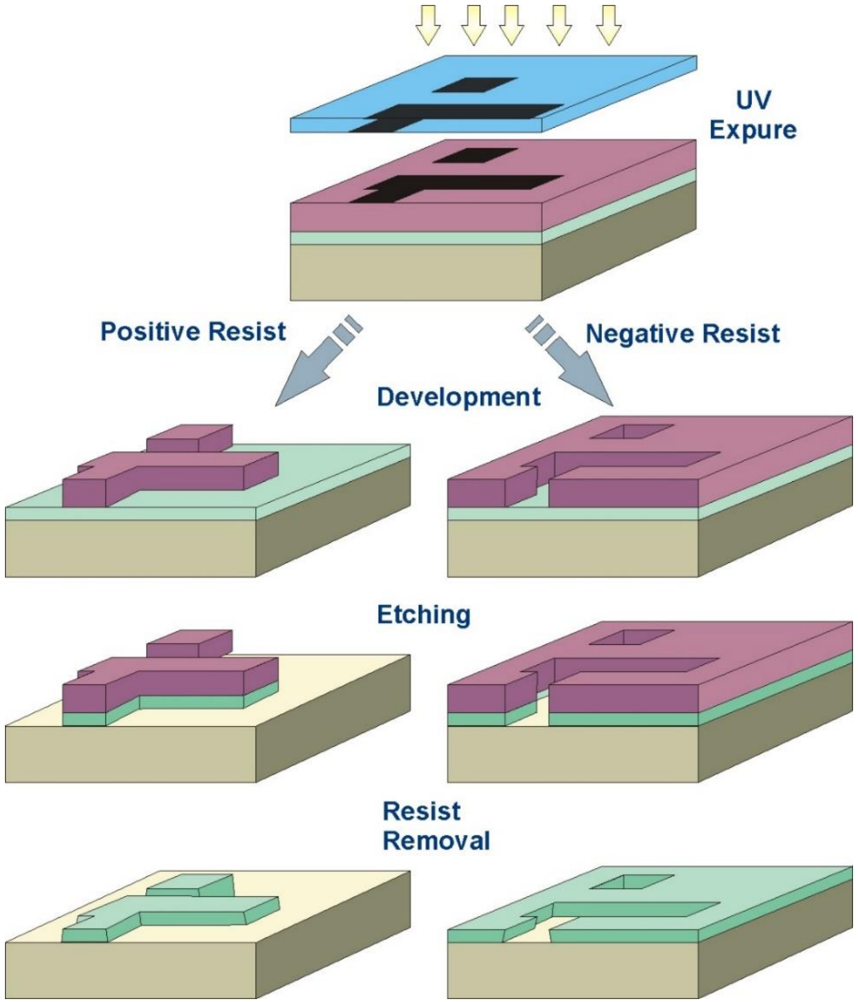
SILICON MICRO- AND NANO-TECHNOLOGIES

ETCHING

It-fab
Italian Network for
Micro and Nano Fabrication

IMM Institute for Microelectronics and Microsystems
Consiglio Nazionale delle Ricerche
BOLOGNA UNIT

Etching is a process by which material is removed from a substrate of from thin films on the substrate surface. When a mask layer is used to protect specific regions of the wafer surface, the goal of the etching is to «precisely» remove the material which is not covered by the mask



There are two fundamental groups of etching:

- **wet etching** (liquid-based etchants)
- **dry etching** (plasma-based etchants, but not only …)

In general an ideal etch process is not completely attainable

Etching processes are not capable of precisely transfering the pattern established by a mask.

PARAMETERS

- **BIAS.** Difference in lateral dimension between the etched image and the mask
- **ETCH RATE**. The rate at which the materiale is removed.
- **SELECTIVITY**. ratio of the etch rates of one materials over the other. For example, the selectivity is ratio of the etch rate of the layer being etched to the etch rate of the mask or the layer under the layer being etched. Etching with high selectivity is supposed to remove the selected layer entirely without harming the substrate and mask.

ANISOTROPY

- Isotropic etching has the same etch rate in all directions.
- Anisotropic etching has different etch rates in the lateral and vertical directions.

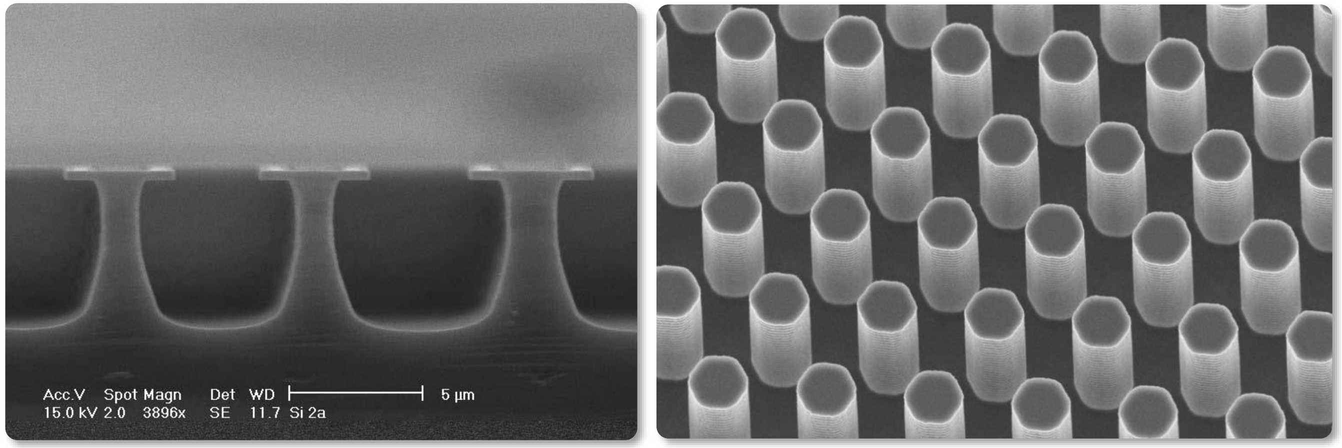
Anisotropic etching is preferable in semiconductor manufacturing processes and for **micro- nano fabrication**. Most wet etching profiles are isotropic, except for etching crystalline materials, whereas etching profiles of dry etching are anisotropic.

Anisotropy is defined as

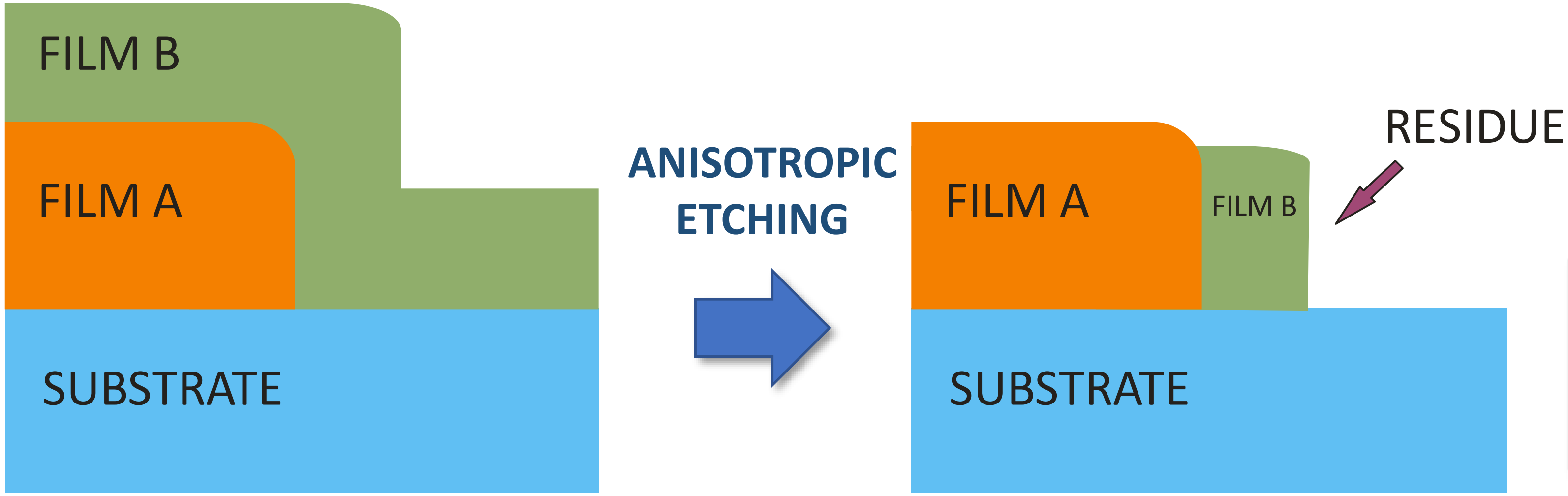
$$A = 1 - \frac{R_L}{R_V},$$

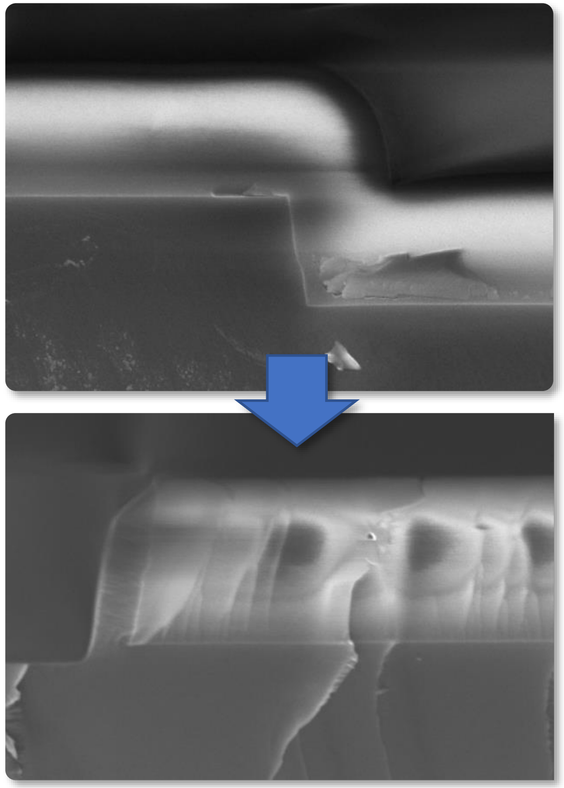
where RL and RV are the lateral and vertical etch rates, respectively. For perfectly anisotropic etching, A is 1. For perfectly isotropic etching, A is 0.

AN EXAMPLE



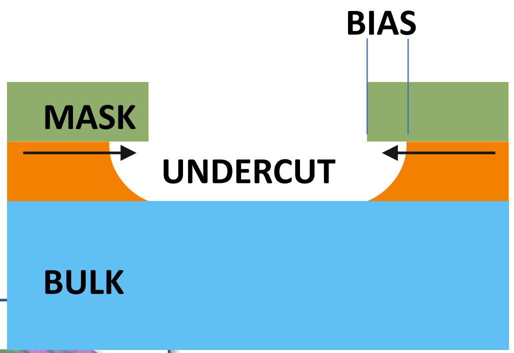
ISOTROPIC (LEFT) AND ANISTROPIC (RIGHT)

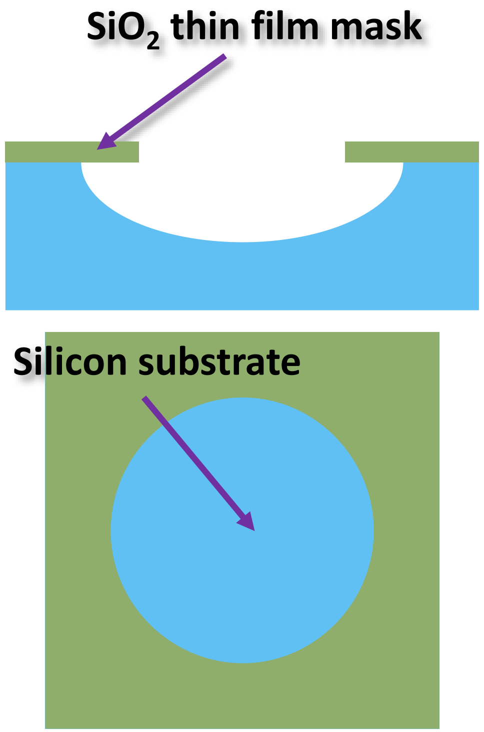


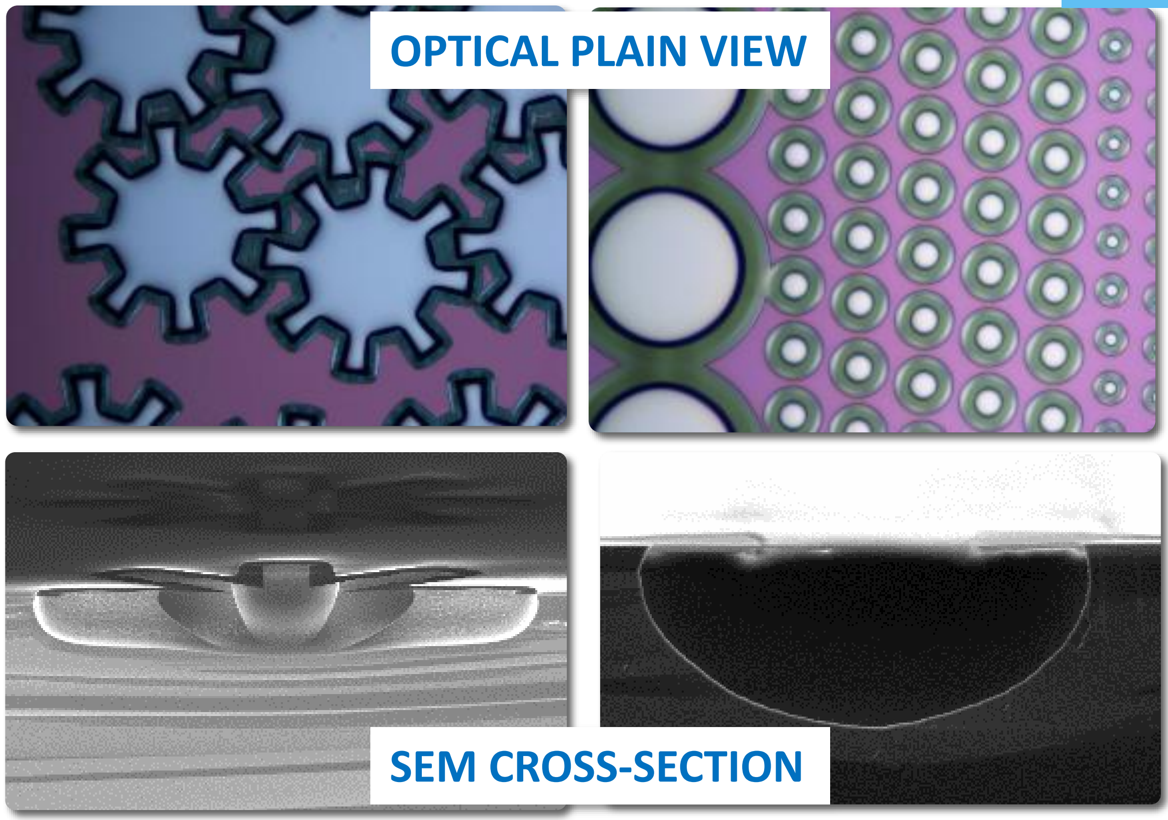


If etching is anistropic, overetching is need to remove residual materials at step

UNDERCUT. Lateral distance per side under the mask, as shown in Figure 1. It can be characterized by the etch rate anisotropy A. Sometimes, the etchant will attack the photoresist pattern, which causes an etch bias.

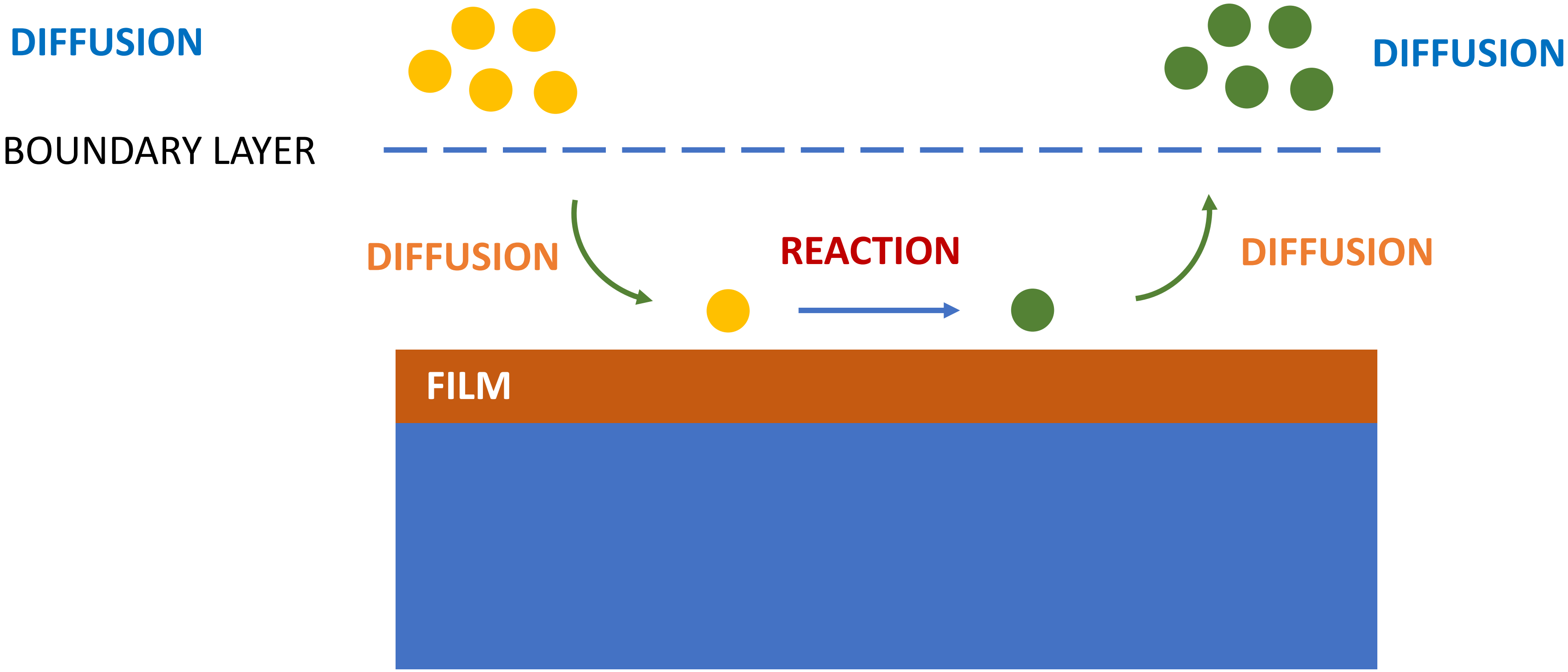






ETCHING PROCESS CONSIST OF THREE STEPS

- Mass transport of reactants (through a boundary layer) to the surface to be etched
- Reaction between reactants and film surface to be etched at the surface
- Mass transport of the reaction products from the surface throught the surface boundary layer



WET ETCHING

- Wet etching was used exclusively till 1970's when **feature size >3um**.
- For small scale features, **large etch bias** leads to significant CD (critical dimension) loss.
- For today's IC industry, wet etching is used for noncritical feature sizes.

ADVANTAGES

high selectivity, relatively inexpensive equipment, batch system with high throughput, etch rate can be very fast (many μm/min).

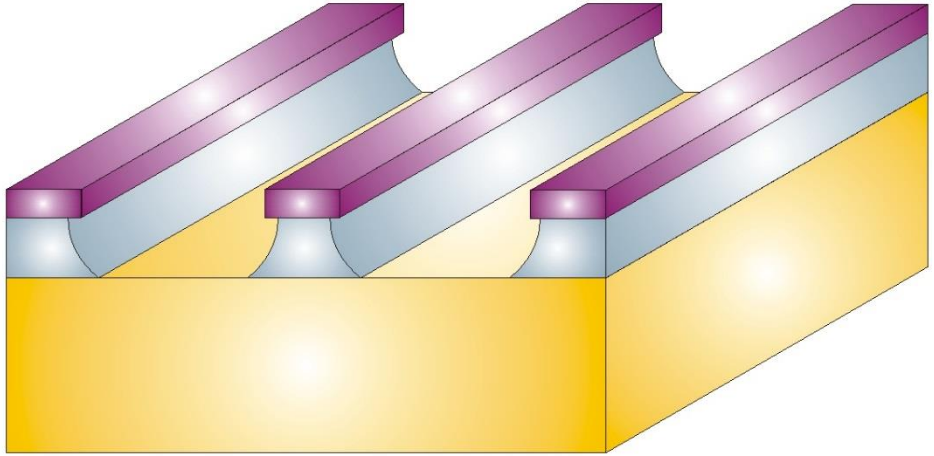
DISADVANTAGES

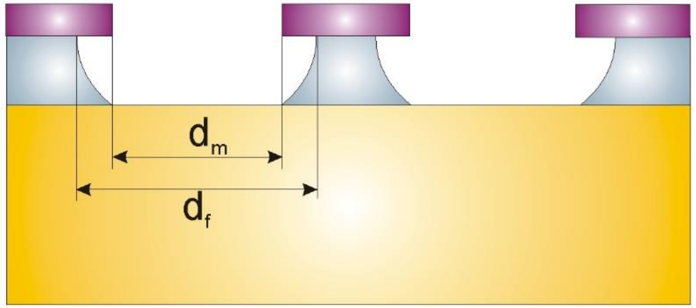
generally isotropic profile, high chemical usage, poor process control (not so reproducible), excessive particulate contamination.

- The etch rate can be controlled by any of the three serial processes: **reactants transport** to the surface (depends on chemical concentration and stirring…), **reaction rate** (depends on temperature), **reaction products transport** from the surface (depends on stirring…).
- Preference is to have **reaction rate** controlled process because
  - Etch rate can be increased by temperature
  - Good control over reaction rate – temperature of a liquid is easy to control
- Mass transport control will result in non-uniform etch rate: edge etches faster.
- Etchant is often stirred to minimize boundary layer and make etching more uniform.

WET ETCHING PROCESS: MAIN MIXTURES

SiO_2	HF, HF + NH_4F
Si_3N_4	BOILING 85% H_3PO_4 @ 180 °C
POLY/SILICON	H_2O+ HNO_3 + HF
ALUMINUM	H_3PO_4+HNO_3+H_2O @ 30 °C
GOLD	KI + I2 + H2O
TITANIUM	HF DILUTED
PLATINUM	H_2O + HCl + HNO_3 (ACQUA REGIA)





SOLVENT CLEANING

- **Methanol, isopropano, acetone Remove organic and metal surface contamination**

PIRANHA SOLUTION

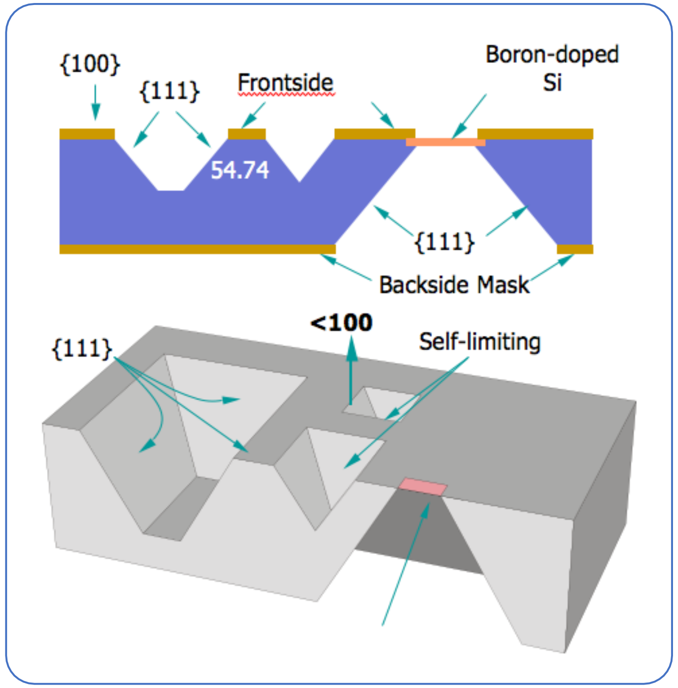
- **$H_2SO_4 + H_2O_2$ Remove organic and metal surface contamination**

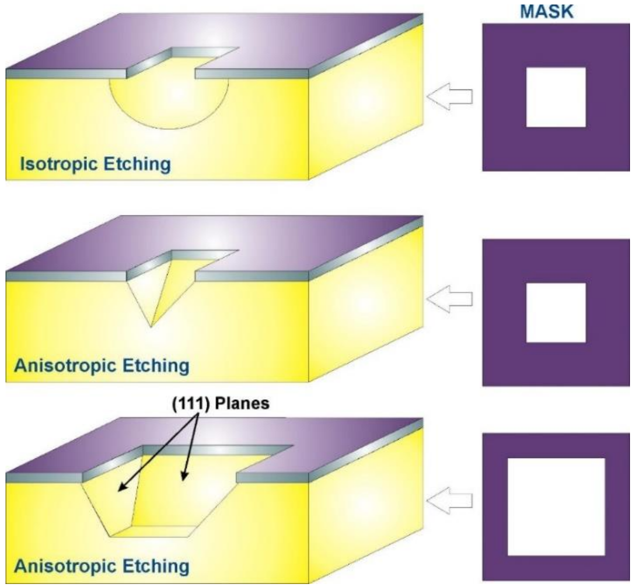
RCA CLEANING

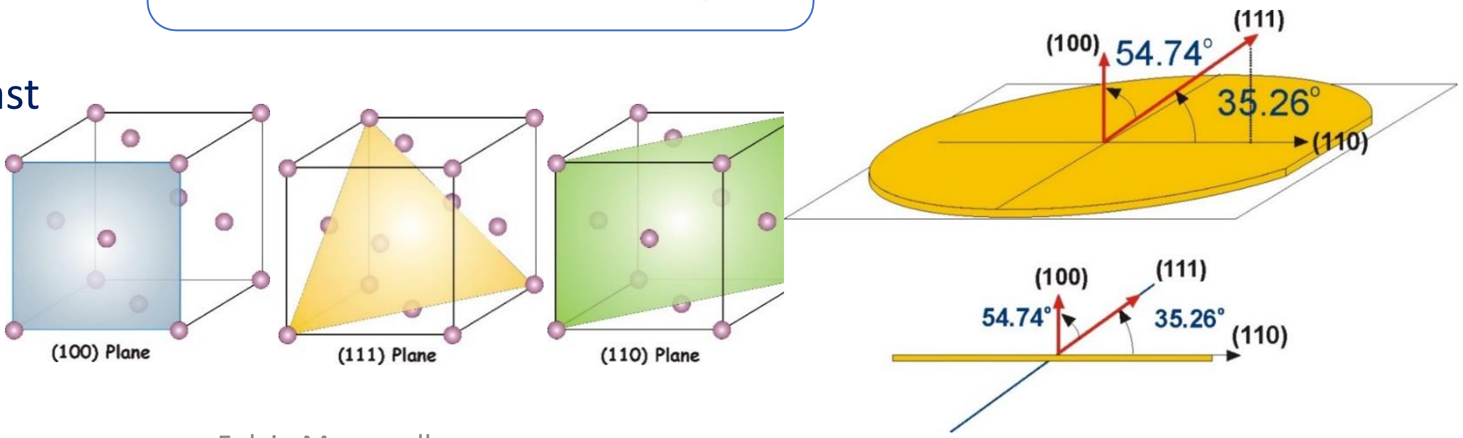
- **$NH_4OH + H_2O + H_2O_2$ Remove organic and particles**
- **$HCl + H_2O + H_2O_2$ Remove metal**
- **$H_2O + HF$**

ETCHING USING ANISOTROPIC AQUEOUS SOLUTIONS RESULTS IN THREE-DIMENSIONAL FACETED STRUCTURE FORMED BY INTERSECTING {111} PLANE WITH OTHER CRYSTALLOGRAPHIC PLANES.

- Orientation selective etch of silicon occur in hydroxide solutions partly because of the closer packing of some orientations relative to other orientations
  - Density of planes: **<111>** > **<110>, <100>**
  - Etch rate: **R(111)** << **R(110)**, **R(100)**
- **<100>** direction etches faster than **<111>** direction, with etch rate
  - **R(100)** = few 100 × **R(111)**
  - It is reaction rate limited
- Used very widely in **MEMS** (micro electro mechanical systems), since it is inexpensive, fast etching and easy to control.







Of the Hydroxides of Alkali metals, **KOH** is by the most common

KOH etches **{111}** plane at a rate 100 times slower than it etches **{100}** plane.

The overall reaction consists of the oxidation of silicon followed of a reduction step:

$$Si + 2OH^- \rightarrow Si(OH)_2^{++} + 4e^- \text{ (oxidation)}$$

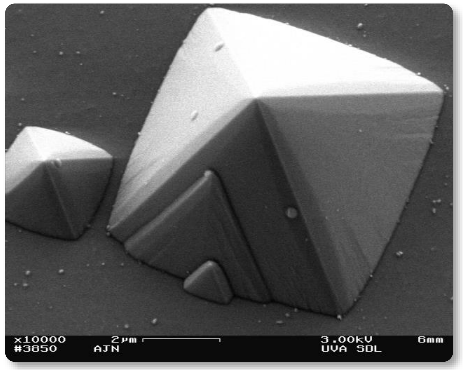
$$Si(OH)_2^{++} + 4e^- + 4H_2O \rightarrow Si(OH)_6^{--} + 2H_2 \text{ (riduction)}$$

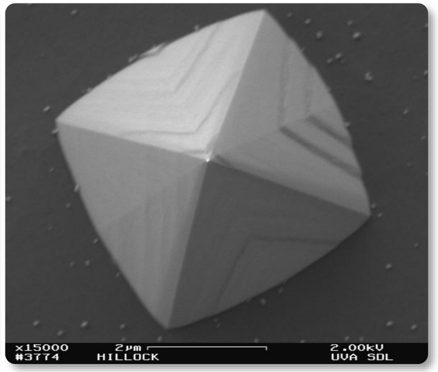
The etch-rate of silicon is approximately 0.5 to 2 µm/min depending on the temperature and concentration of KOH. It is also selective to heavily doped p-type silicon (p++), making common the use p++ doping as etch stop.

Due to the presence of alkali metals inside the etchant, it gives the solution

not CMOS compatible!

- TMAH (**($(CH_3)_4NOH$)**) etches **{111}** plane at a rate 30 to 50 **slower** than **{100}** plane.
- The etch rate drops by a factor 40 in heavily p-doped silicon
- A disadvantage of TMAH is the occasional formation of undesirable pyramidal **hillock** at the bottom of the etched cavity.

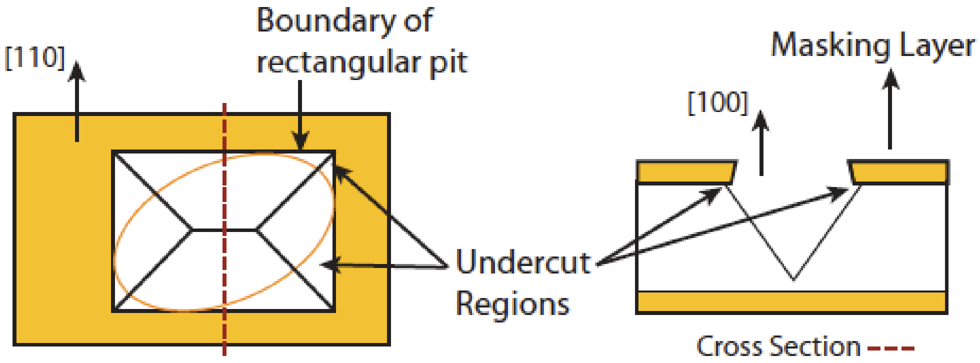




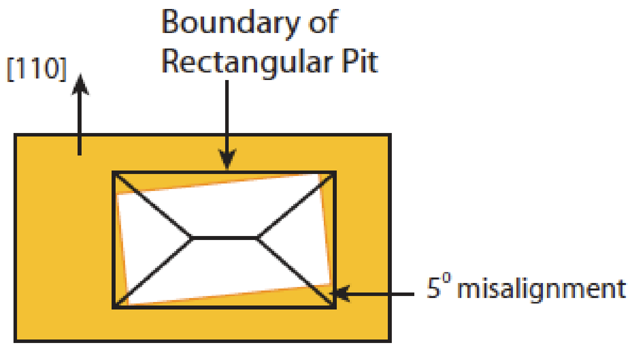
- Both **silicon dioxide** and silicon nitride remain virtually unetched in TMAH, and hence can be used as **masking layers**.
- It is advisable to **remove native silicon oxide** in HF acid prior to etching in TMAH
- TMAH is an organic material, so it does not contain any metal ions, making TMAH a potentially **IC-compatible** etching agent.

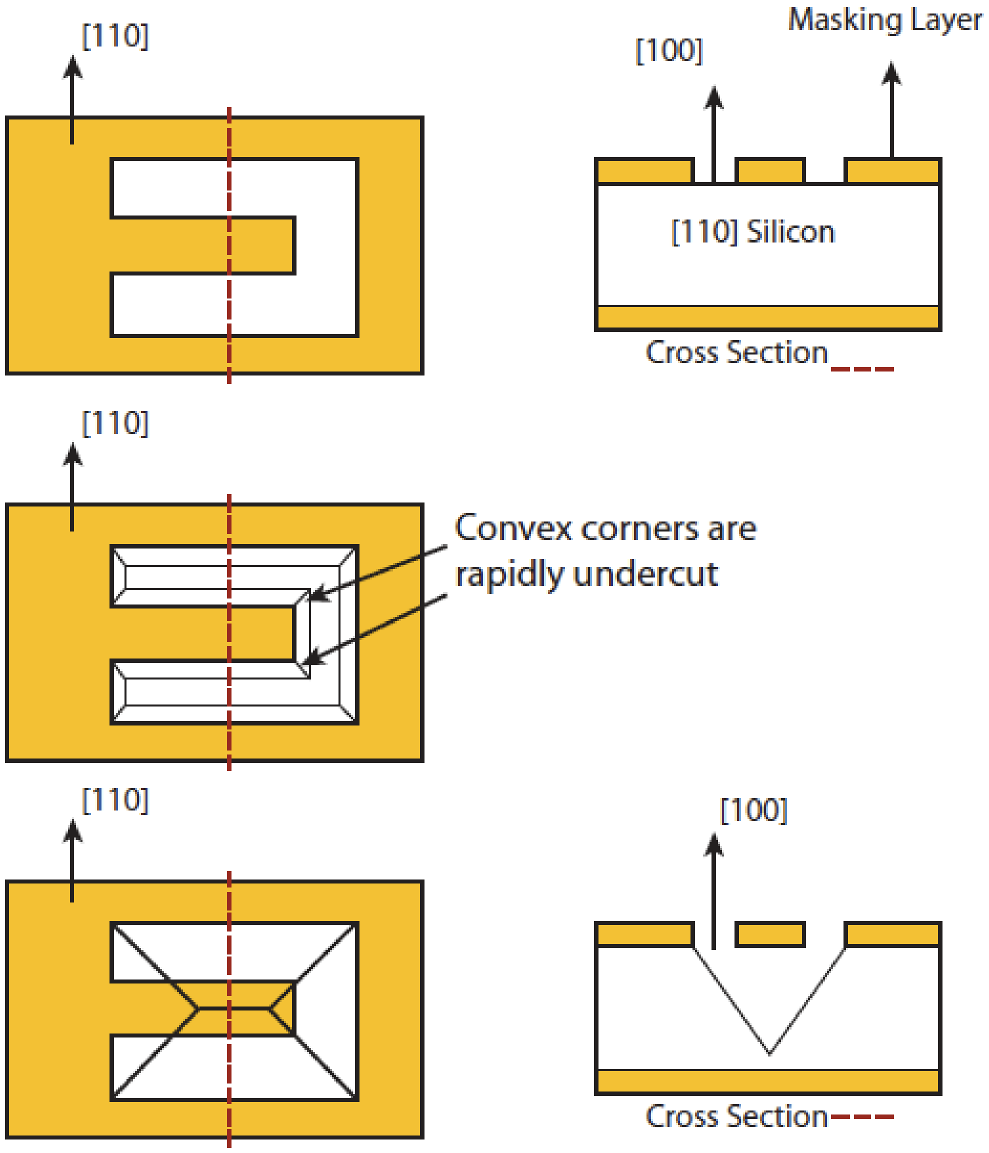
	ETCH STOP	ETCH RATE (100) µm/min	ETCH RATE RATIO (100)/(111)	REMARKS	MASK
KOH	**B > 10^{20} cm^{-3}** REDUCED ETCH RATE BY 20	**1,4**	**100**	IC INCOMPATIBLE, ETCHES OSIDE FAST LOTS OF H_2 BUBBLES	**Si_3N_4, SiO_2**
TMAH	**B > $4 \cdot 10^{20}$ cm^{-3}** REDUCED ETCH RATE BY 40	**1**	FROM **12.5** TO **50**	IC COMPATIBLE, Easy to handle	**SiO_2** etch rate is 4 orders of magnitude lower than (100) silicon **Si_3N_4**

Any mask feature, if etched long enough, will result in a V-groove tangent to the mask along <110> directions

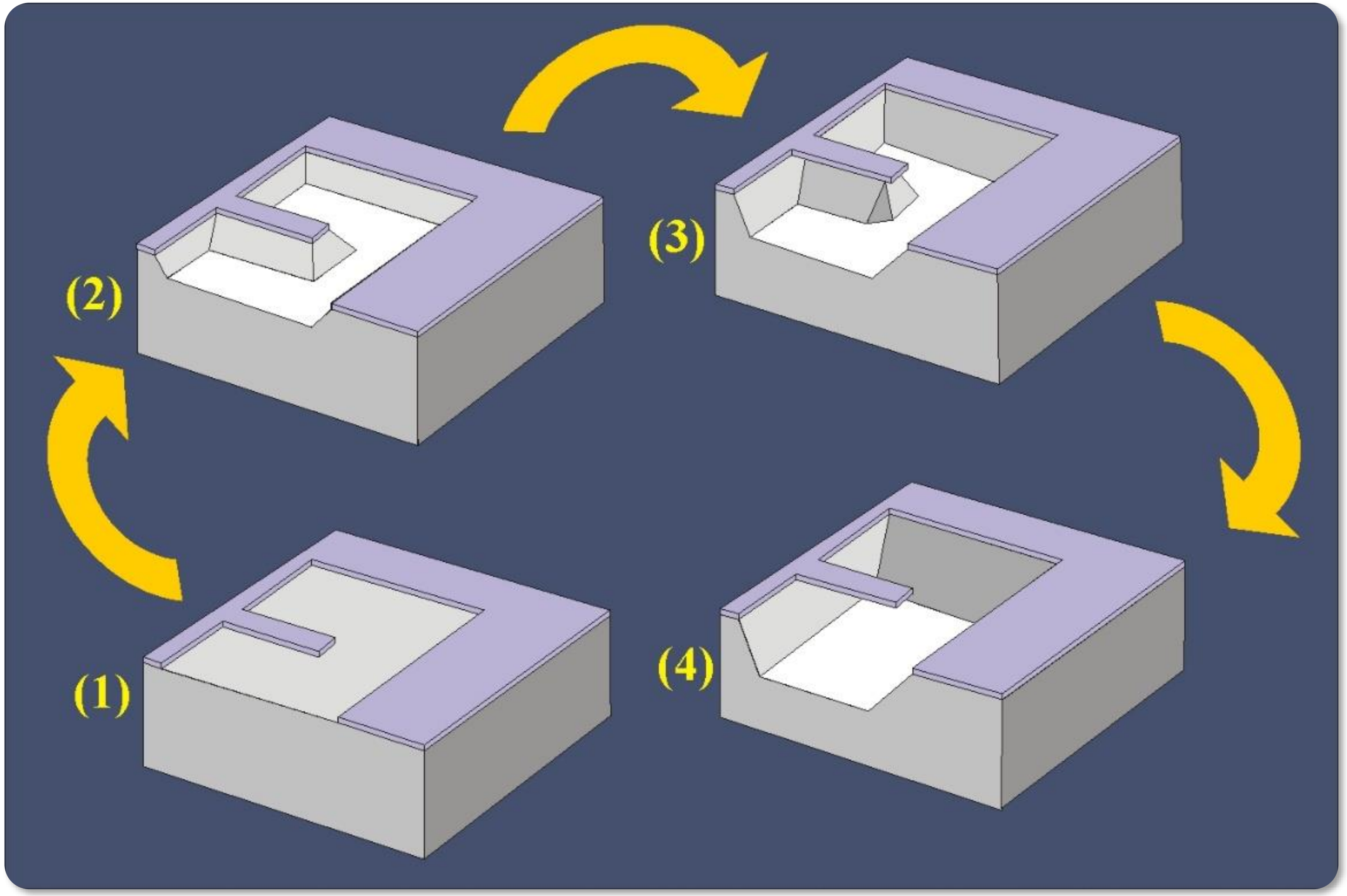


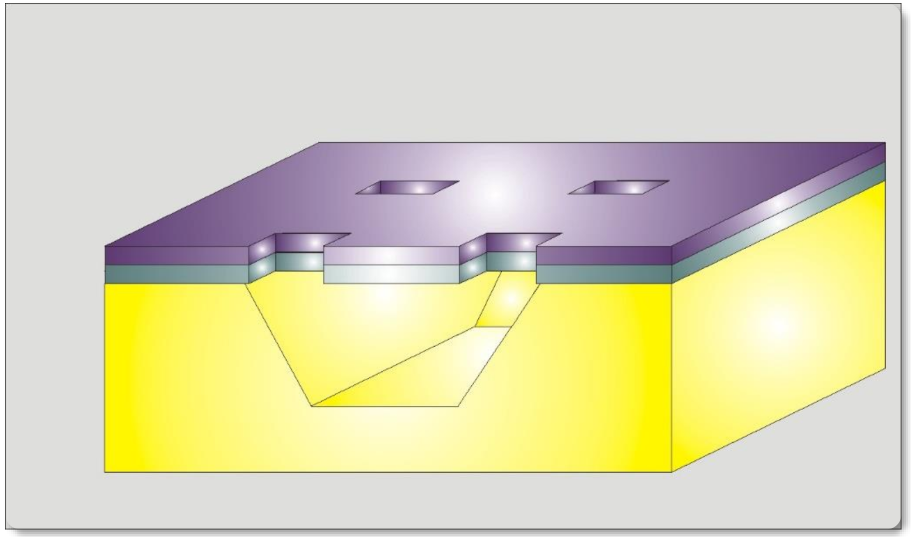
Misalignment of the mask relative to the [110] direction always results in a larger etched region





TMAH ETCHING: Simplified process flow for the realization of a cantilever



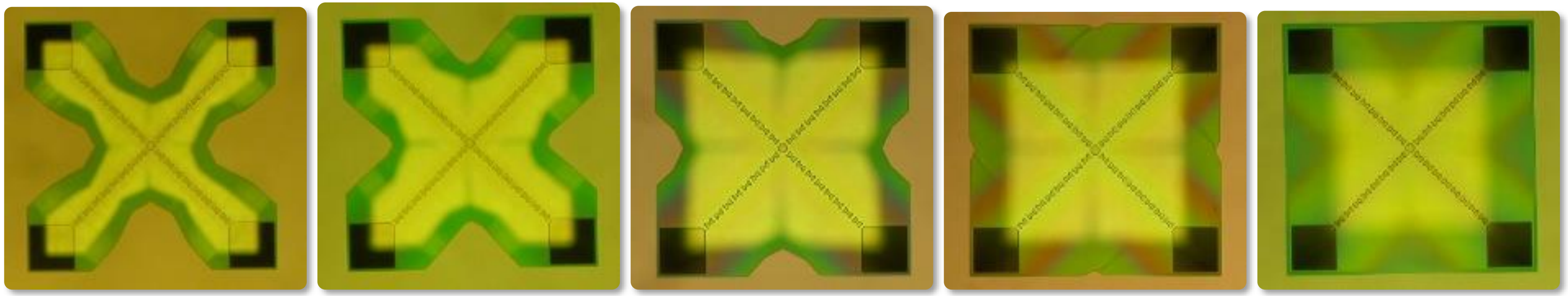


Deposition of membrane stack

Lithography to define the membrane

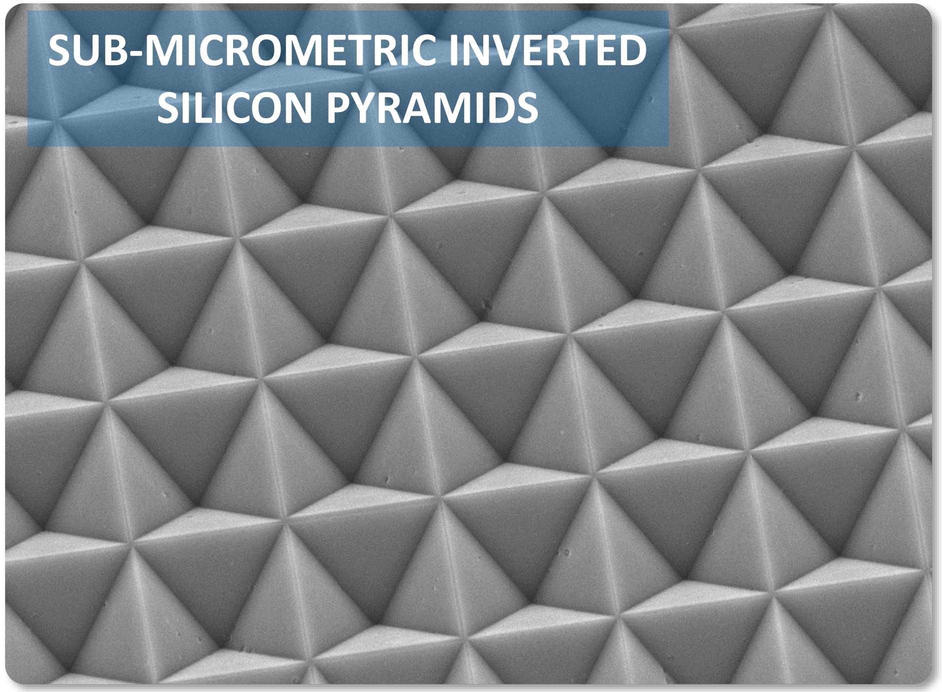
Etching to realize the holes in the membrane stack

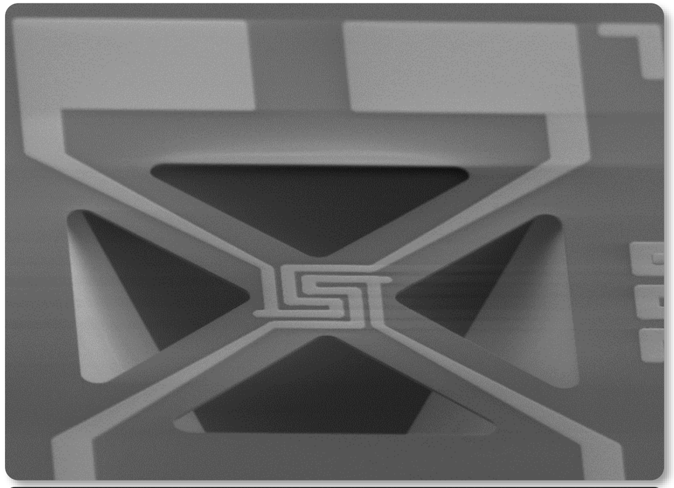
Anisotropic Wet silicon etching

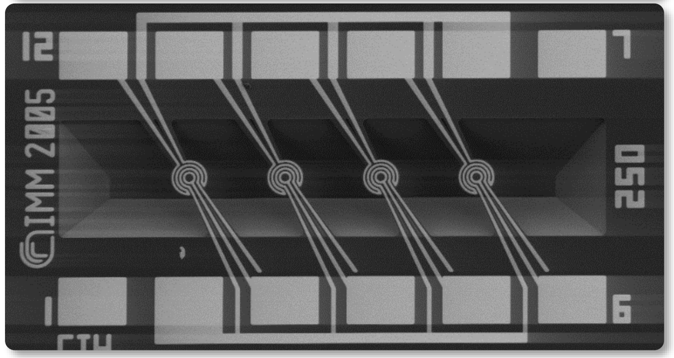


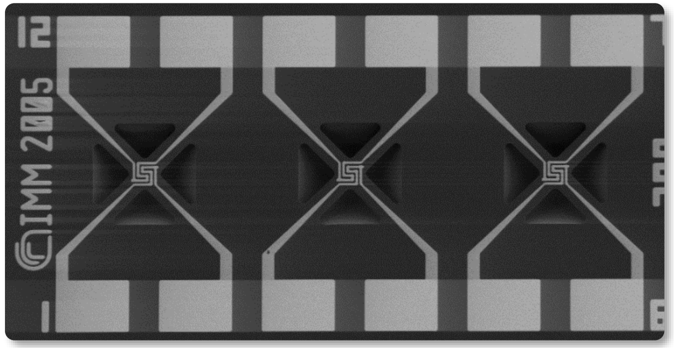
120 min 150 min 180 min 225 min 300 min

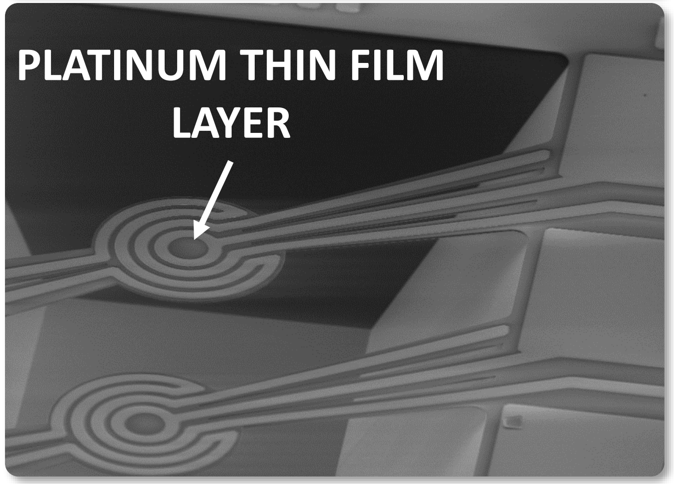
TMAH ETCHING: SEM IMAGES STRUCTURES AND SUSPENDED MEMBRANE WITH DIFFERENT GEOMETRIES

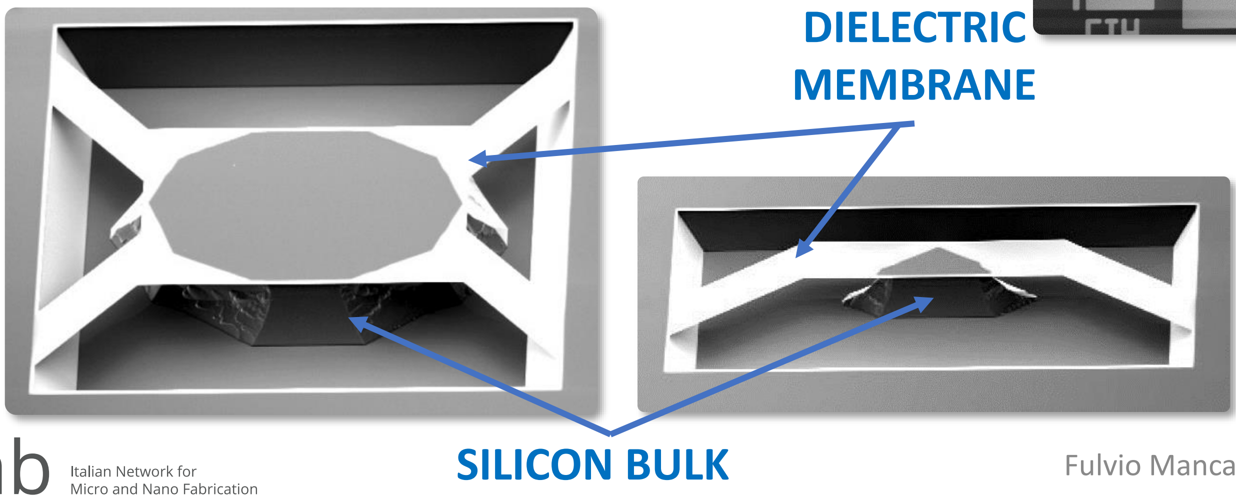


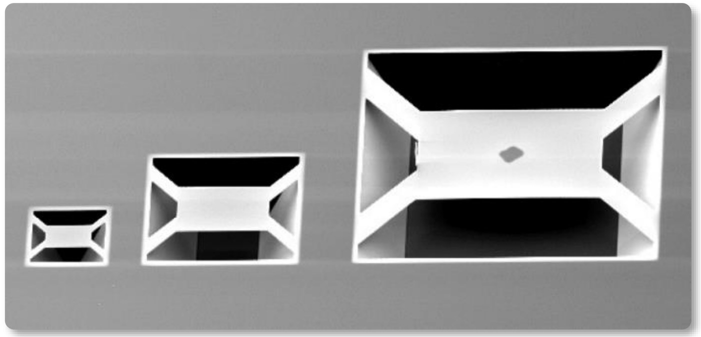












The procedure of transfering patterns onto a wafer by wet etching was ***well established***, and the liquid etchant systems are available with very high selectivity .

However, wet etching processes are typically **isotropic**. Therefore, if the thickness of the film being etched is comaprable to the minimum pattern dimension, undercutting due to isotropic etching become intollerable.

One alternative pattern transfer method that offers the capability of non-isotropic (*anisotropic*) etching is «***dry etching***».

A considerable effort has been expected to develop dry etch processes as replacements for the wet etch process.

The overall goal of an *dry etch process* for VLSI/MEMS fabrication is to be able to reproduce the features on the mask with fidelity.

This should be achiveable with control of

- *Slope* of the feature sidewalls
- *Degree* of undercutting

In addition a useful etch process should have the following characteristics:

1. Highly selective against etching the mask layer material
2. Highly selective against etching the material under the film being etched
3. Etch rate should be rapid
4. Etch uniforme across the entire wafer
5. Cause minimal damage
6. Mask material should be easily removed
7. Process should be clean

A VARIETY OF DRY ETCH PROCESS TYPES EXIST

HIGHER EXCITATION ENERGY

PHYSICAL SPUTTERING

- Physical momentum transfer
- Directional etch (anisotropic) possibile
- Poor selectivity
- Radiation damage possible

RIE – REACTIVE ION ETCHING

- Physical (ion) and chemical
- Directional
- More selective than sputtering

PLASMA ETCHING

- Chemical
- Isotropic
- More selective
- Less prone to radiation damage

HIGHER PRESSURE

Dry etch processes based on a combination of physical and chemical mechanisms offer the potential of controlled anisotropic etching, toghether with adeguate selectivity

PHYSICAL ETCHING

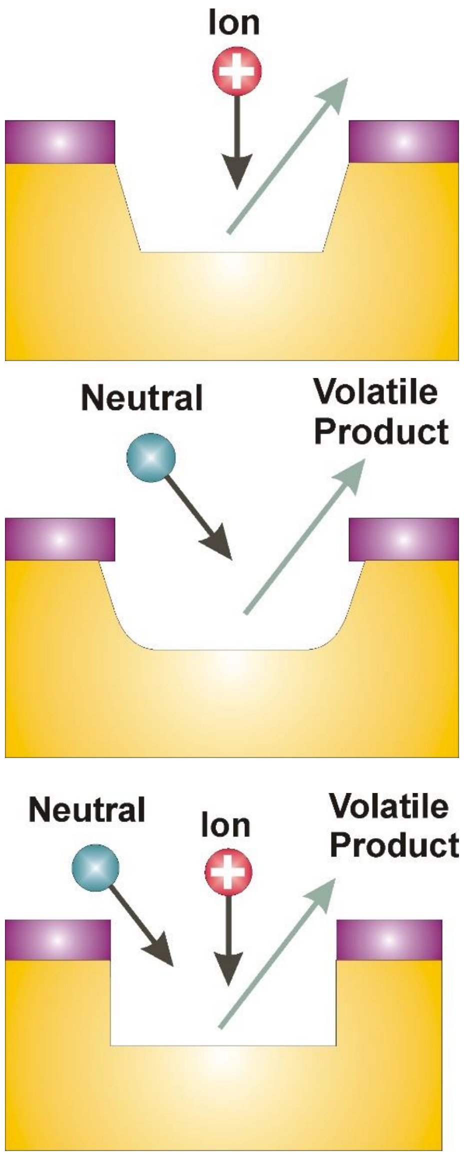
positive ions are accelerated and strike substrate with high kinetic energy, some energy is then transferred to surface atoms, which leads to material removal.

CHEMICAL ETCHING

neutral or/and ionized species interact with the material's surface to form volatile products. Chemical etching mechanisms typically etch in a isotropic fashion.

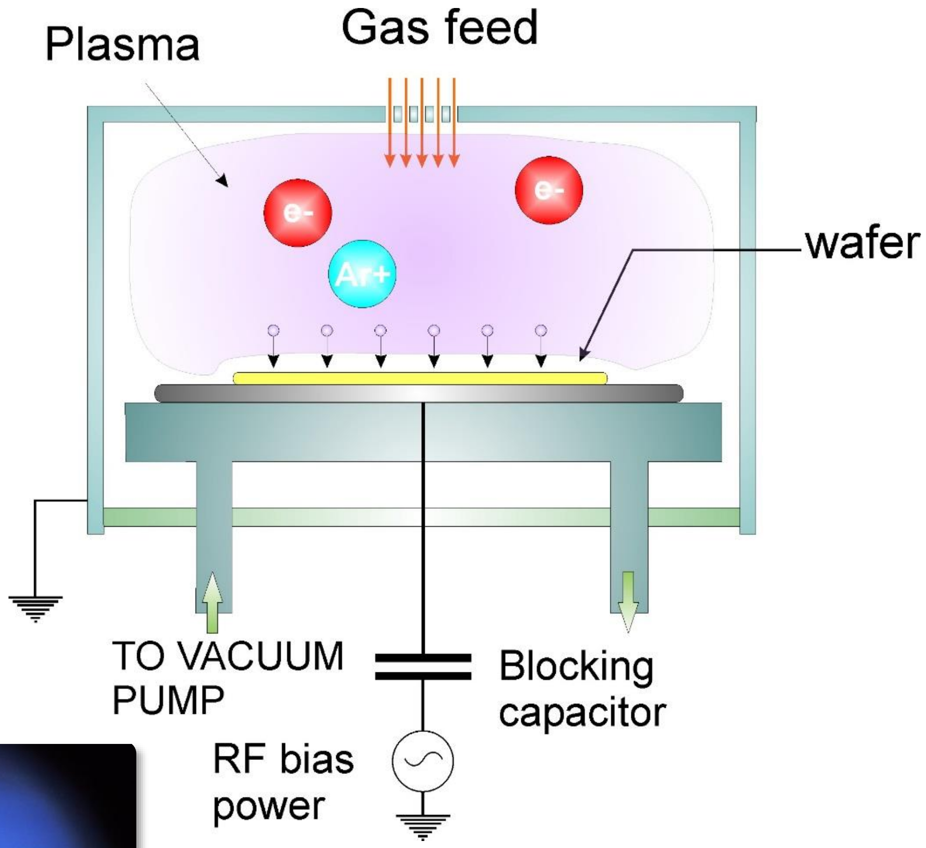
Combination of Chemical and Physical etching (Reactive Ion Etching - RIE)

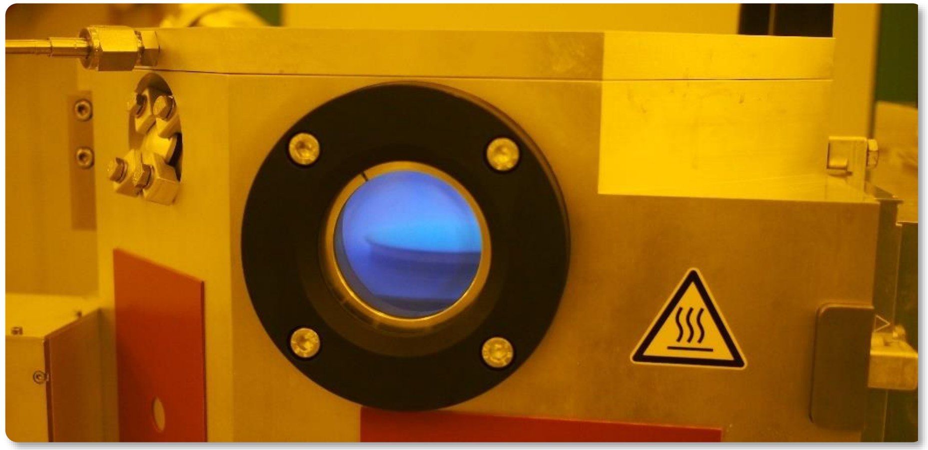
An anisotropic profile is obtained

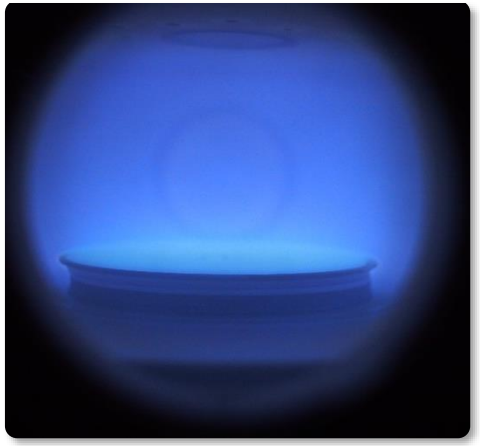


A plasma is fully or partially ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules.

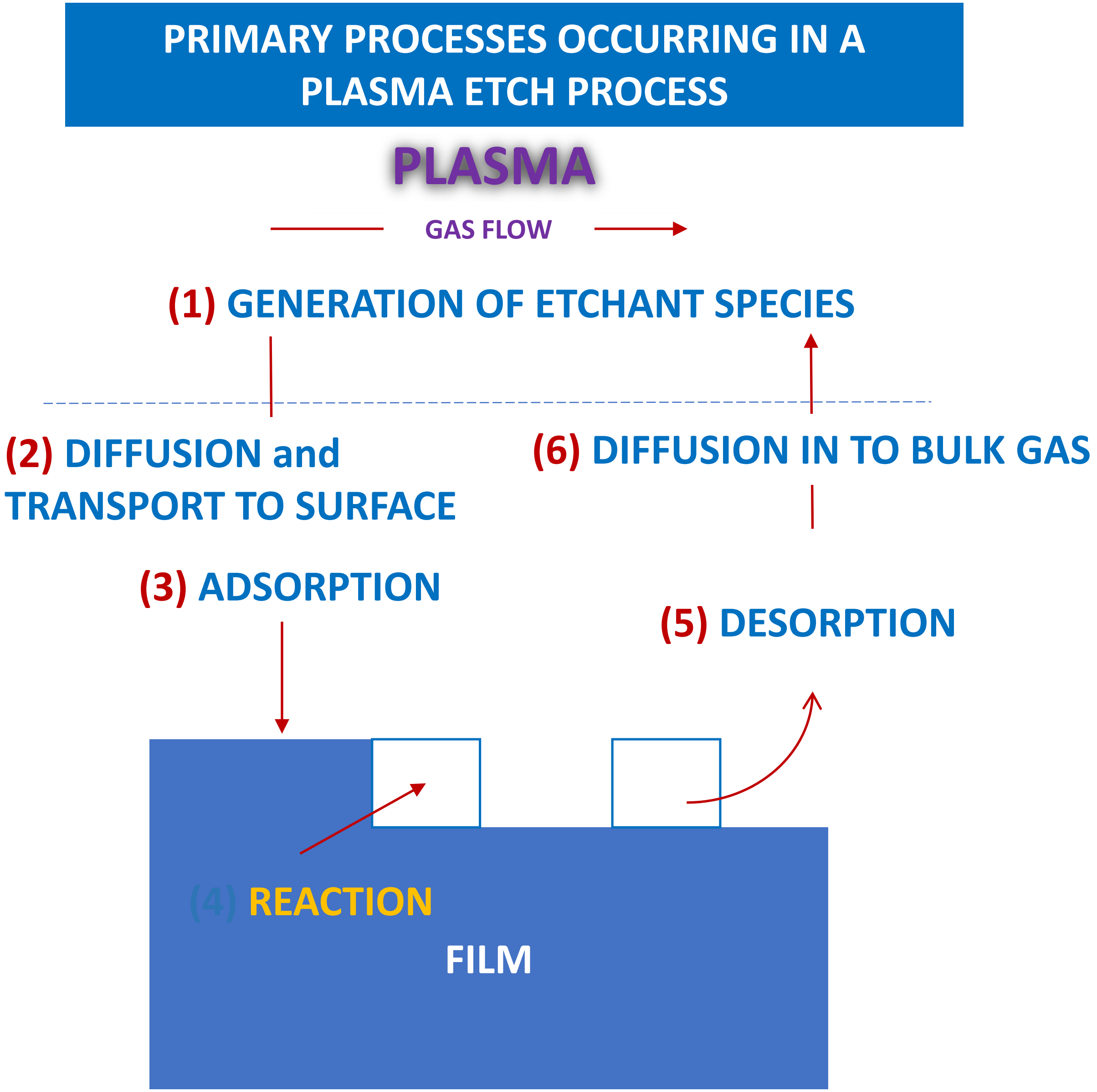
A plasma is produced when an electric field of sufficient magnitude is applied to a gas, causing the gas to break down and become ionized.







An ideal dry etch process based on chemical mechanism can be broken down in to six steps.



The basic concept of plasma etching is rather direct.

1. A glow discarge is utilized to produce chemically reactive species (atoms, radicals, and ions) from a relatively inert molecular gas (or mix of gases)
2. The etching gas is selected so as to generate species which react chemically with the material to be etched,
3. and whose reaction product with the etched material is **volatile**.

Etching directionality is due to direction energy input into an etching reaction at a surface and can be accomplished by **neutral**, **ion** (i.e. RIE), **electron** and **photon** bombardment of a surface exposed to a chemical etchant.
Plasma etching can be divided in two main groups:

ION-INDUCED RIE→ reaction-controlled etching

ION-INHIBITOR RIE → desorption-controlled etching

ION-INDUCED RIE

Technique used when the substrate is not etched spontaneously: ions modified the surface reactions in one way or another (e.g. chemical sputtering, chemical enhanced physical sputtering) and make it possible for radical to react with the substrate

e.g: Cl_2/Si

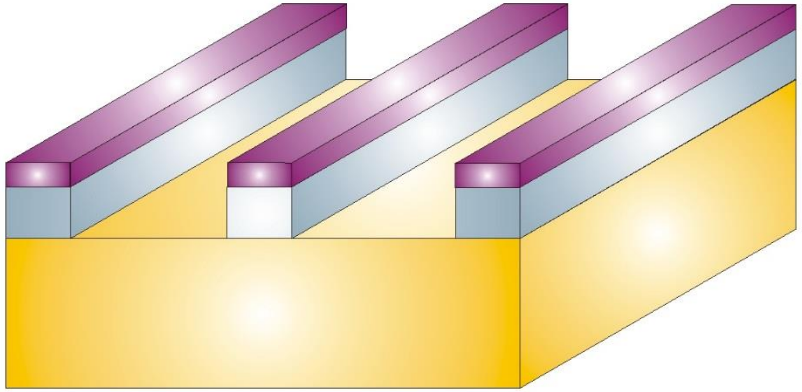
ION-INHIBITOR RIE

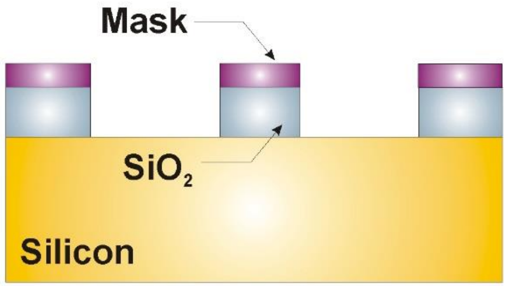
The substrate is etched spontaneously and an **inhibiting layer** is need to achieve directionality.
Sidewalls of thences are not exposed to ion bombardment . The botton of the trench is exposed to ion bombardment thus free from this deposit and etching can proceed.
Passivation layer can be grown by:

- inserting gases which act as silicon oxidant (Anisotropy < 1)
- Inseting gases which act as polymer precursor (thermally instable)
- Freezing the normally volatile reaction product (cryogenic system)
- Erosion and redeposition of mask material (contamination)

e.g: F/Si, Cl_2/Al

MATERIAL	ETCH GASES	ETCH PRODUCTS
SILICON/POLYSILICON	$SF_6 + O_2$ $SiCl_4$ $Cl_2 + BCl_3$	SiF_4 $SiCl_4$ $SiCl_4$
SiO_2	$CHF_3 + Ar$ $CF_4 + H_2$	$SiF_4 + CO_2$ $SiF_4 + CO_2$
Si_3N_4	$CHF_3 + Ar$ $CF_4 + H_2$ $SF_6 + O_2$	$SiF_4 + NO_x$
ALUMINUM	$Cl_2 + BCl_3$ $Cl_2 + HBr$	$AlCl_3$, Al_2Cl_6
ORGANIC	O_2, CF_4	CO, CO_2, HF



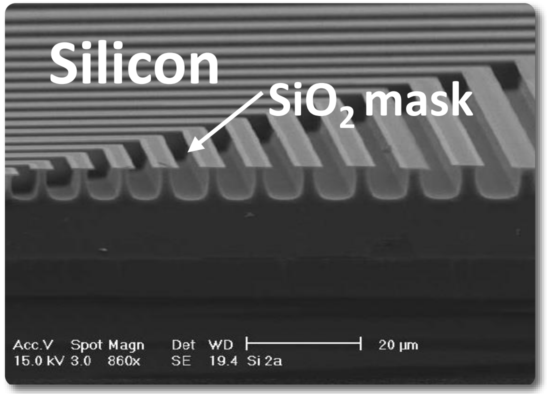


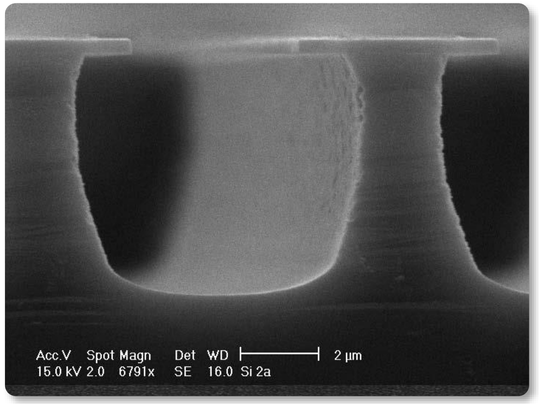
ION-INHIBITOR RIE

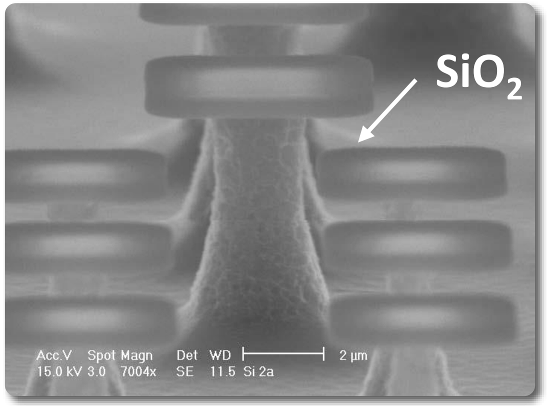
GASES: SF_6, O_2

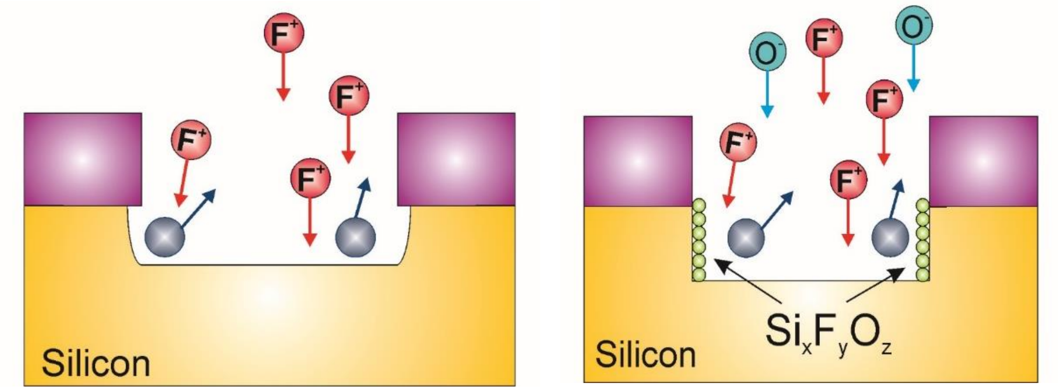
SF_6: substrate is etched spontaneous

O_2: Act as Si oxidant (Passivation layer)

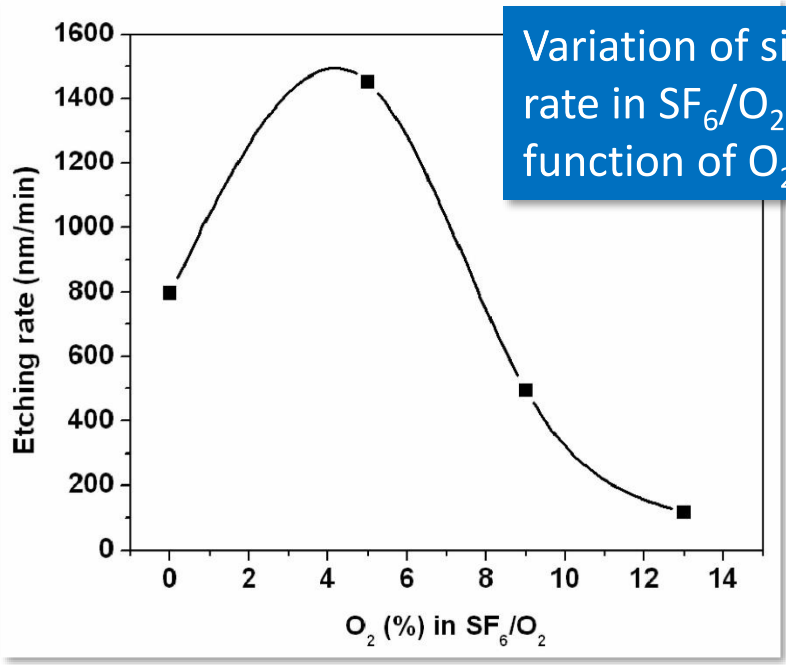








$Si_xF_yO_z$ inhibitor layer

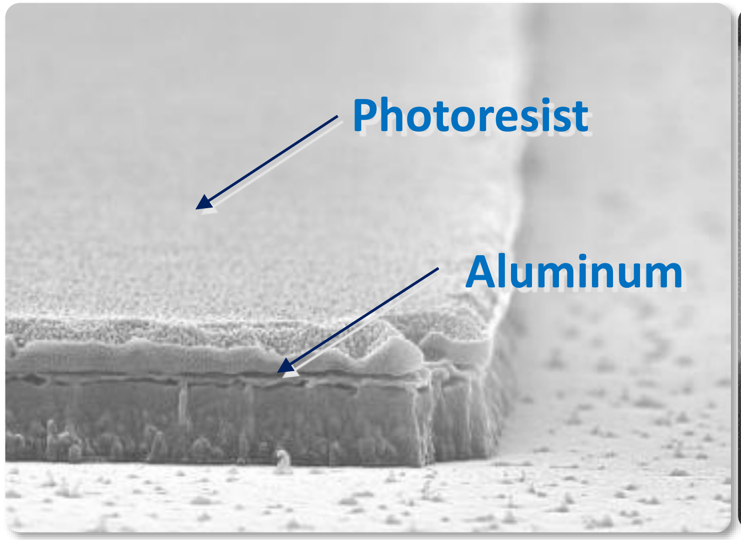


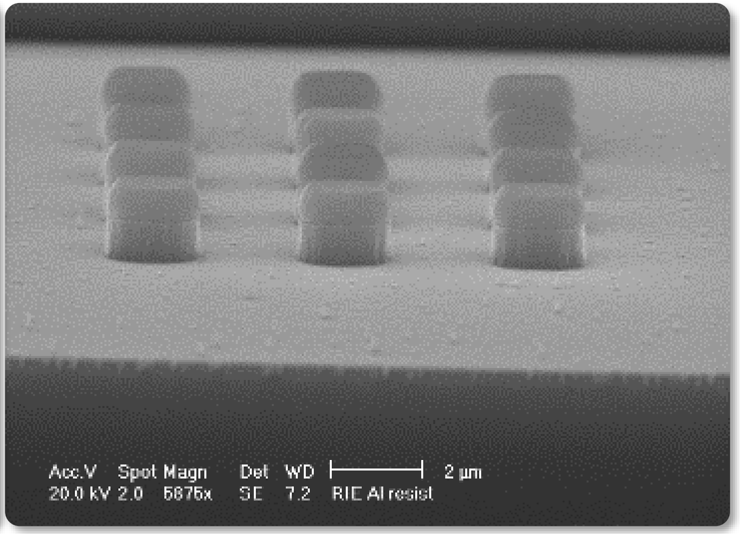
Variation of silicon etching rate in SF_6/O_2 plasma as a function of O_2 percentage

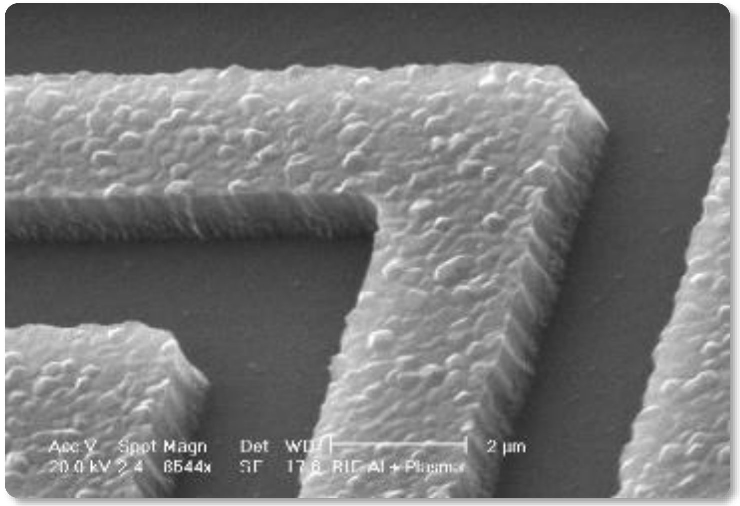
The SF_6/O_2-Si system is an ion-inhibitor process. In this gas system oxygen covers the silicon surface with silicon oxide and the SF_5^+ ions etch the passivation layer making it possible for the F* radicals to etch the silicon substrate.

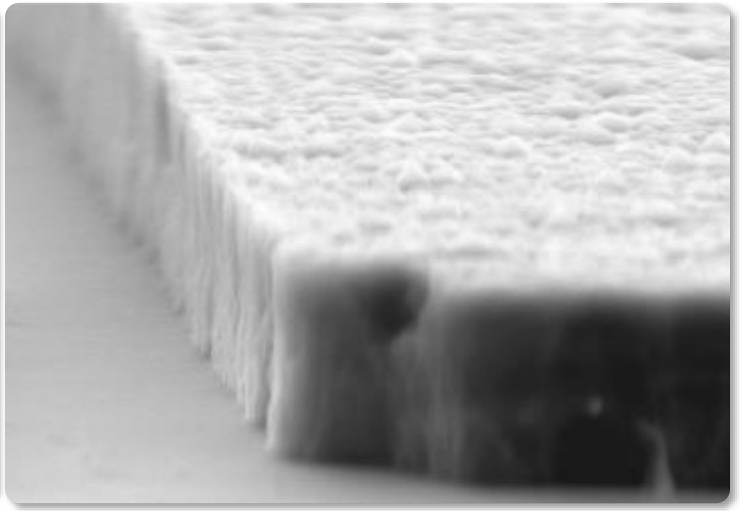
Mat. Res. vol.21 no.5 São Carlos 2018 Epub July 10, 2018

CHLORINE-BASED PLASMA: THIN FILM ALUMINUNM DRY ETCHING









ION-INHIBITOR RIE

Passivation layer

- Erosion and redeposition of mask material

GASES: Cl_2, BCl_3, Ar

BCl_3: to remove fastly and reproducibly the aluminium oxide layer

Cl_2: enhances the etch rate of the aluminium

Ar: Stabilizes the plasma

- **Aluminum is spontaneously etched by Cl_2**
- **Surface of aluminum is always protected by a native aluminum oxide layer a few nanometers thick**
- **Ion bombardment is essential for Al etching**

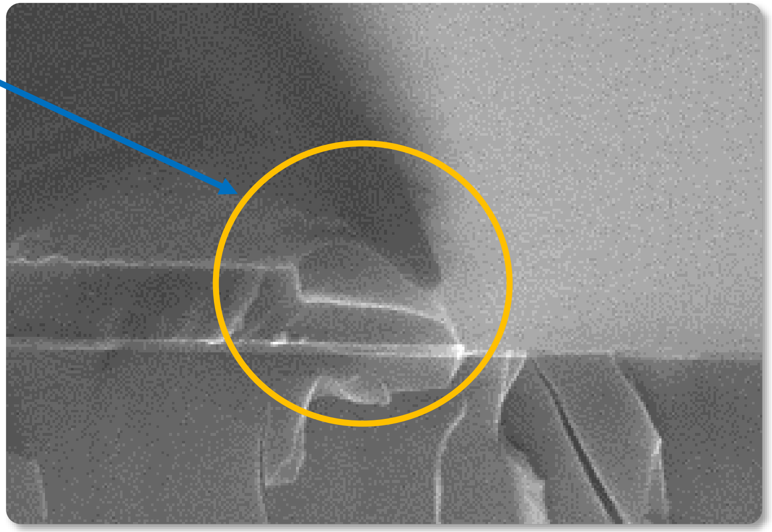
ION-INDUCED RIE

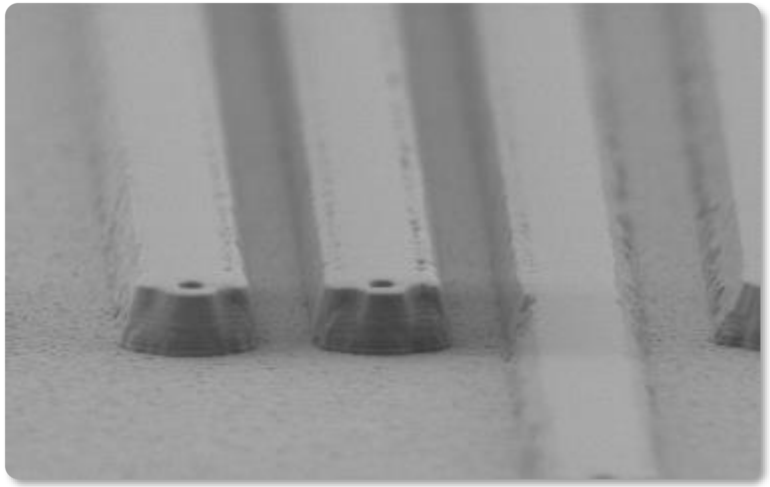
Passation layer

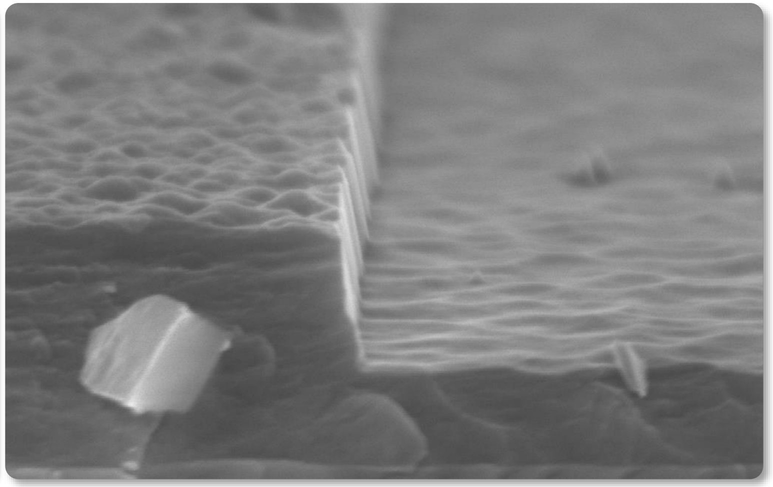
- Erosion and redeposition of mask material

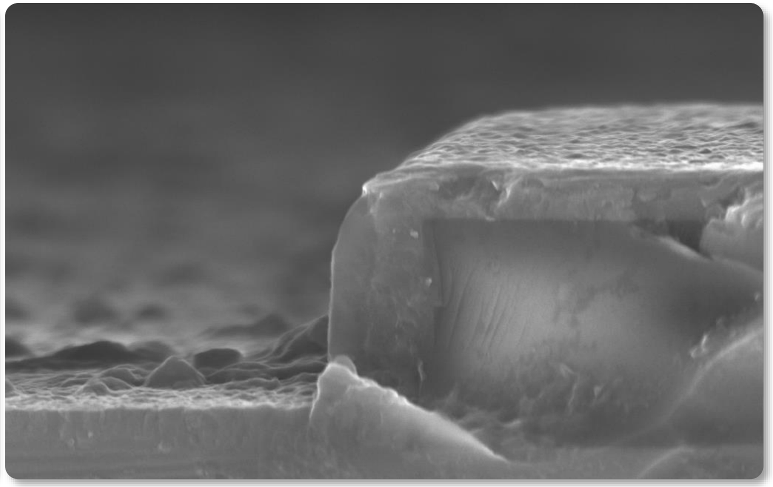
GASES: $SiCl_4$
ETCH PRODUCT: $SiCl_4$

Problem: excess passivation.
The sidewall profile is not vertical



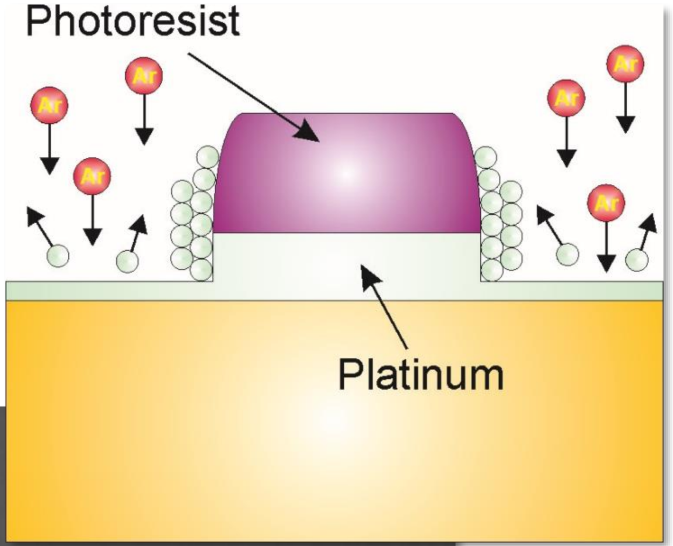


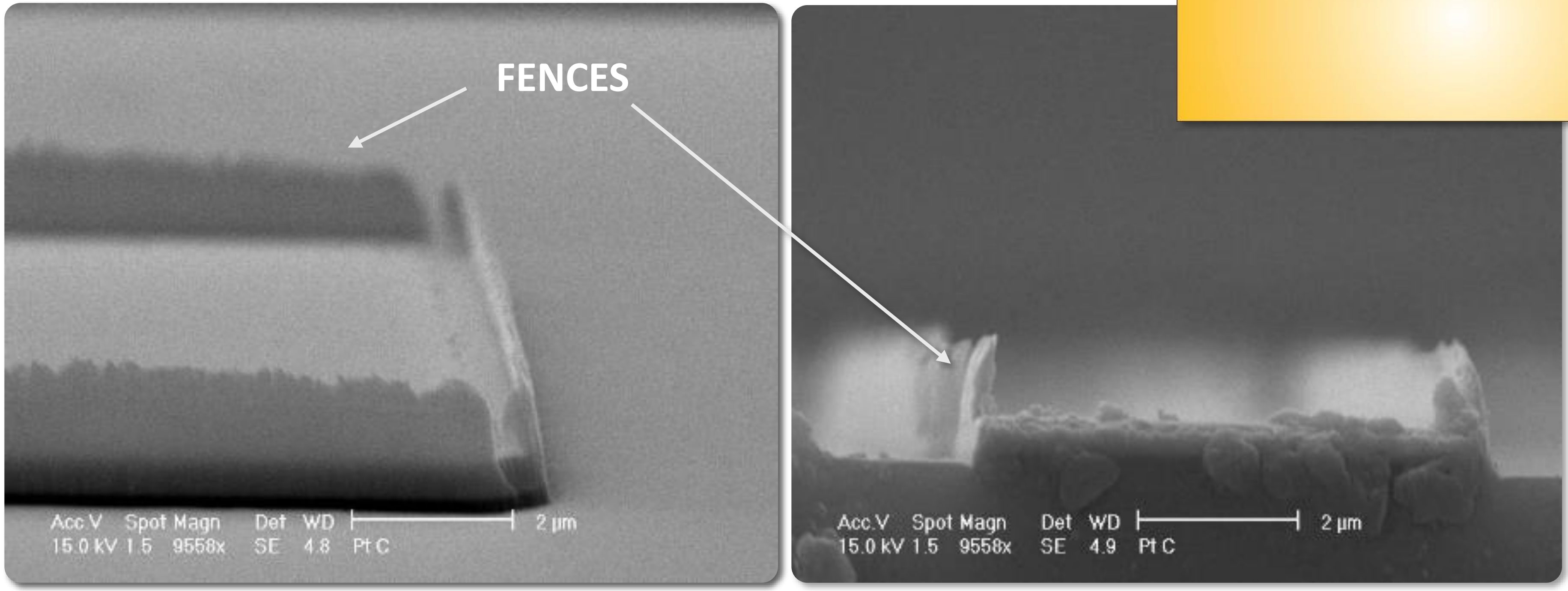




- Platinum has been physically etched by argon plasma.
- The fences are due to platinum redeposited on the sidewall.

GASES: Ar





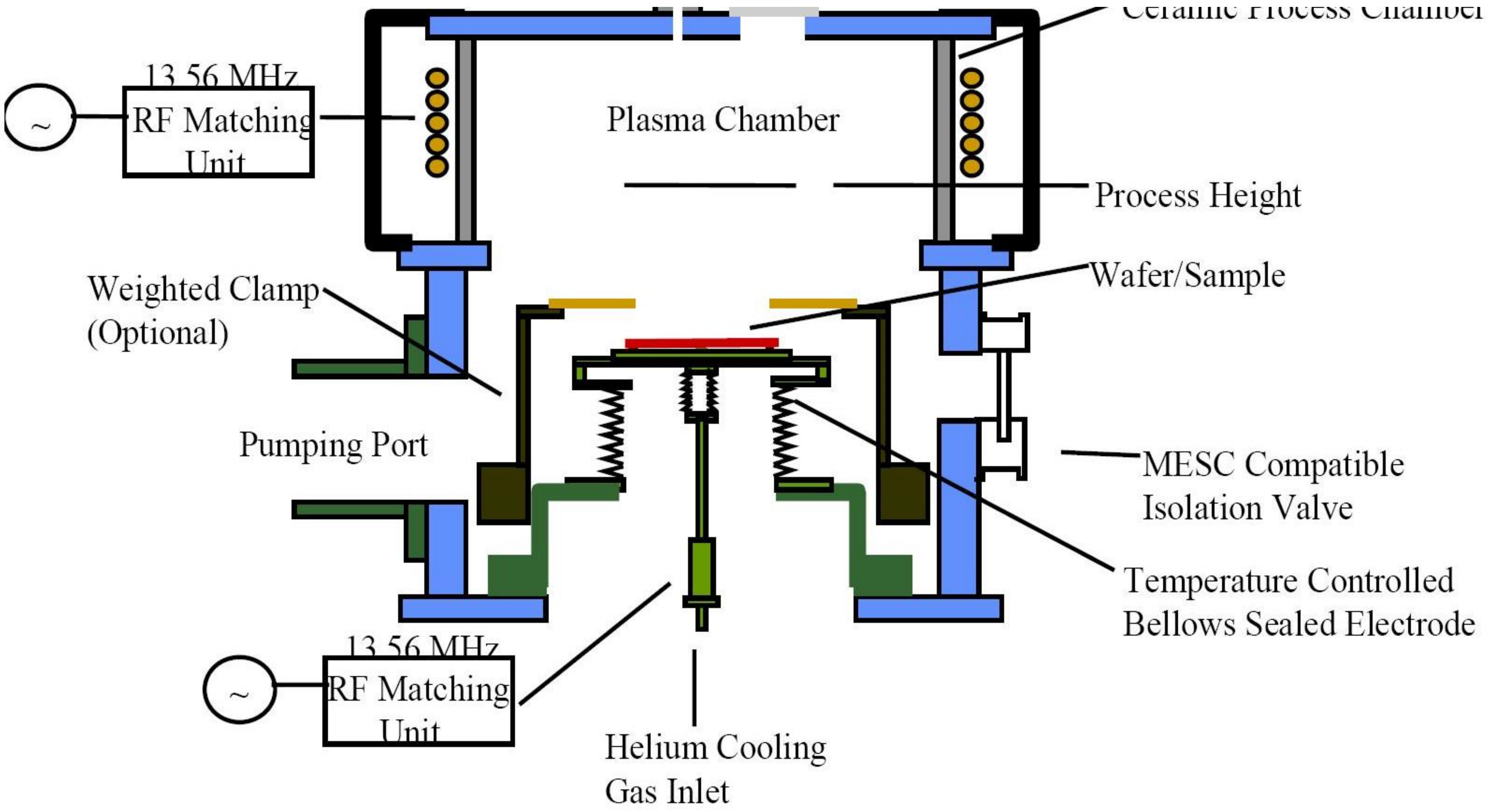
RIE (CCP - capacitively coupled plasma) are able to etch silicon and other material slowly

How to increase the etch rate?

INCREASING THE DENSITY OF PLASMA

Inductively Coupled Plasma (ICP) RIE
In this type of system, the plasma is generated with an RF powered magnetic field. Very high plasma densities can be achieved

A combination of parallel plate and inductively coupled plasma RIE is possible. In this system, the ICP is employed as a high density source of ions which increases the etch rate, whereas a separate RF bias is applied to the substrate (silicon wafer) to create directional electric fields near the substrate to achieve more anisotropic etch profiles



13.56 MHz
RF Matching Unit
Plasma Chamber
Process Height
Weighted Clamp (Optional)
Wafer/Sample
Pumping Port
MESC Compatible Isolation Valve
Temperature Controlled Bellows Sealed Electrode
13.56 MHz
RF Matching Unit
Helium Cooling Gas Inlet

There are two main technologies for high-rate DRIE

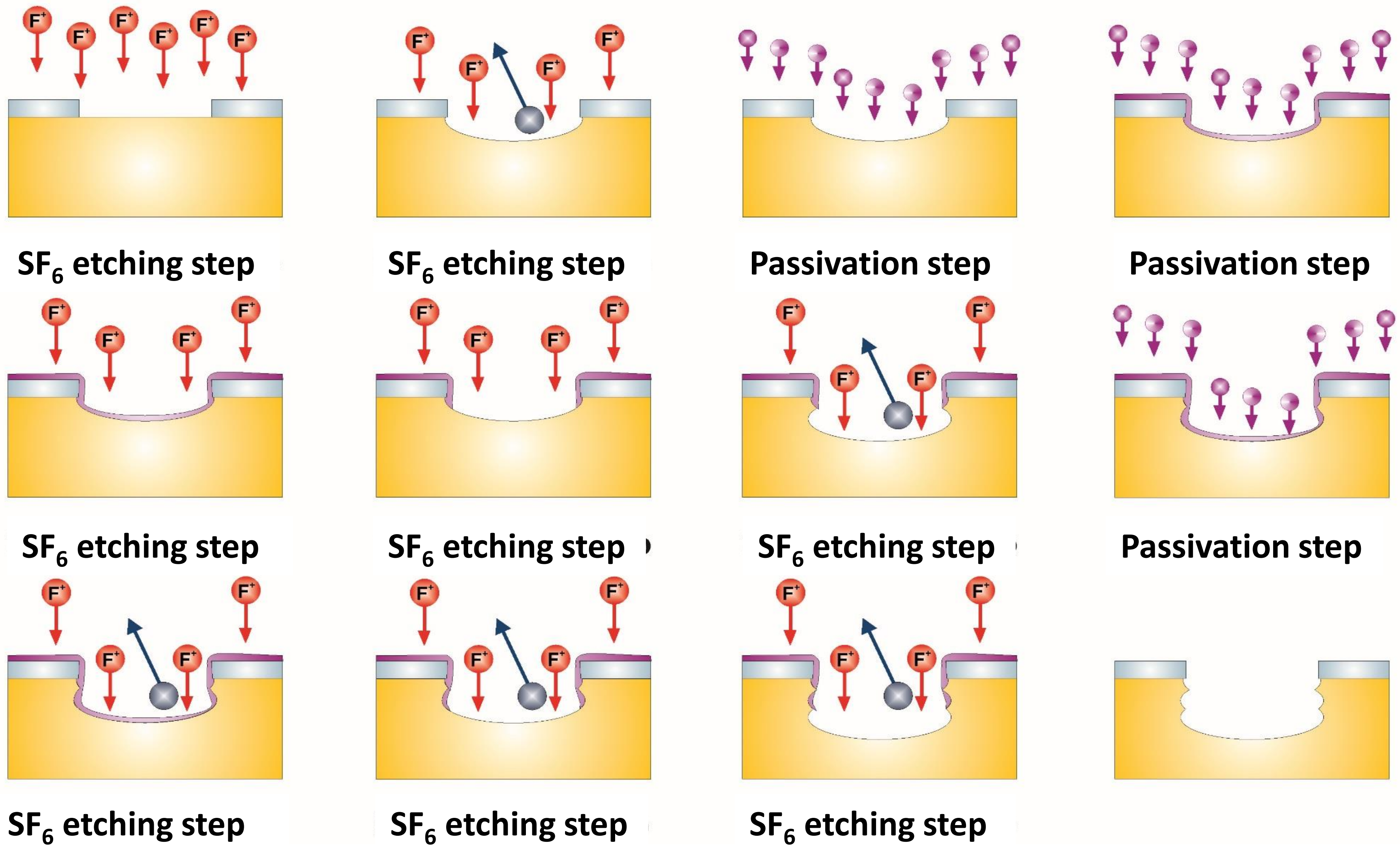
BOSCH PROCESS

Anisotropic reactive ion etching involves the delicate balance between passivation of the sidewalls and etching of the bottom of the structures. The etch is mainly produced by bombardment of ions from the plasma discharge. Lærmer and Schilp first developed this etch technique at Bosch and hence it is also commonly referred to as the "Bosch process." This technique involves alternating etch and passivation steps in a continuous cycle to achieve the high aspect-ratio structures. Both steps are done at room temperature

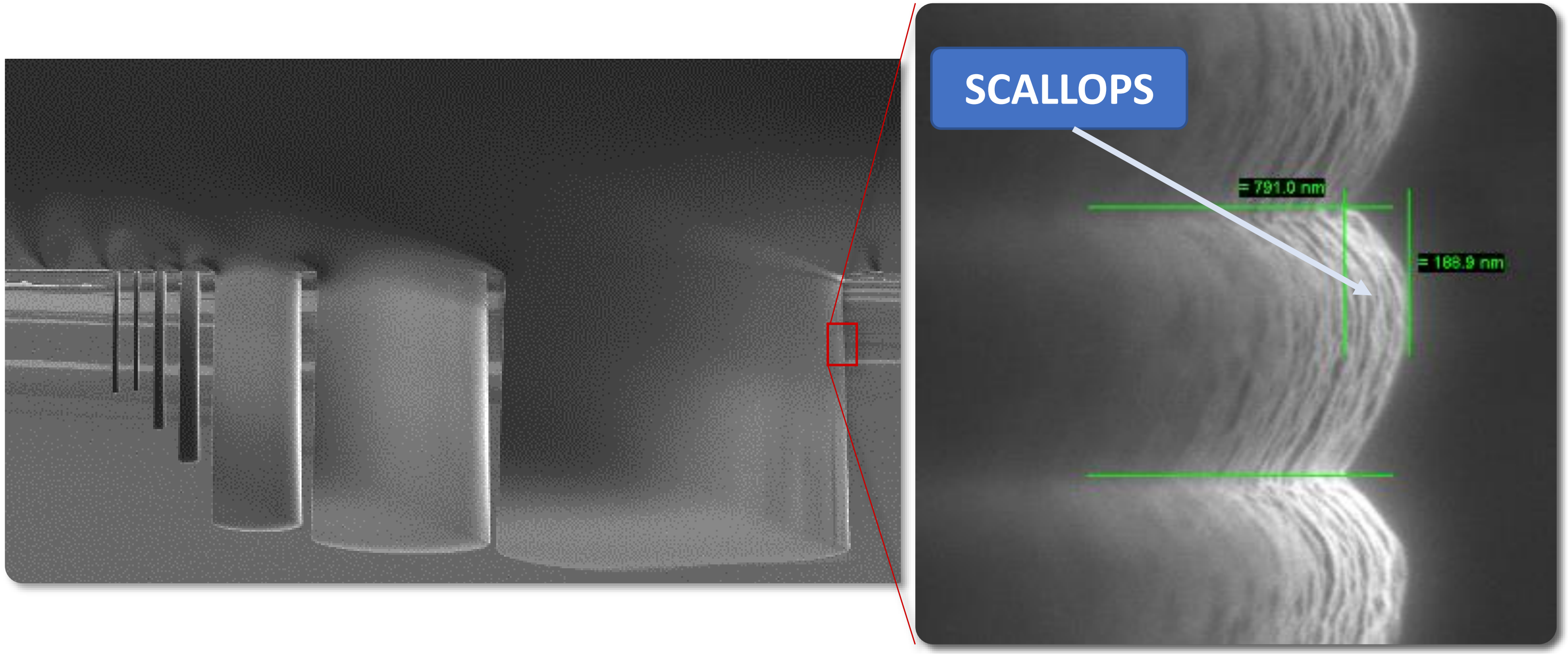
CRYOGENIC PROCESS

An alternative technique introduced by Tachi *et al*. involves etching substrates at cryogenic temperatures, also using fluorine-based high-density plasmas. The main chemical reactions that occur in reactive ion etching are those due to spontaneous etching and those due to ion-assisted reactions. The spontaneous reactions which occur on both the sidewalls and the bottom account for the isotropic etch. To produce anisotropic etches the spontaneous reaction has to be slowed considerably. Tachi *et al*. accomplished this by controlling the substrate temperature, the rationale being that cooler temperatures will reduce the reaction probability or the incident flux of radicals on the sidewalls

BOSCH PROCESS: PRINCIPLE



Surface roughness issues are particularly important in BOSCH tools. Because of alternate etching and passivating cycles and the spontaneous nature of the etch in fluorinated chemistries, structures fabricated using BOSCH process exhibit a characteristic scalloped sidewall roughness that can be unacceptable in some applications.
It is possible to minimize the depth of those scallops by varying the operation conditions during dry processing. The depth of the scallops is due mostly to the spontaneous etching of silicon by fluorine.



MACRO-LOADING

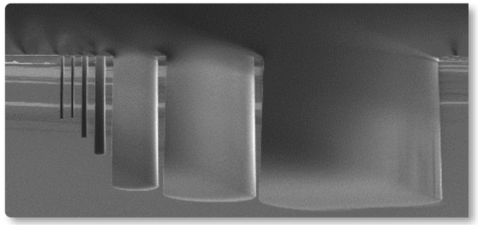
Etch rate for a given process becomes slower with more exposed etch area

- Etch rate is limited by the arrival of neutrals (neutral limited regime)
- Is a function of total exposed area reacting with gas phase species
- Center to edge uniformity variations can be a result of macro loading

MICRO-LOADING AND RIE LAG

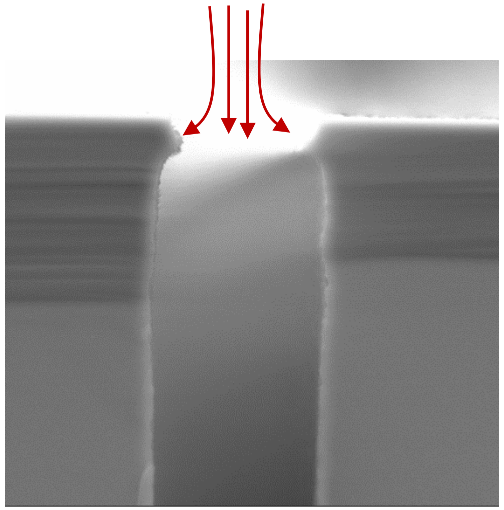
Smaller features etch slower than larger features.

Gas conductance indeep narrow holes is low and the reactants simply can not reach the bottom effectively (or the reaction products removed). Ion bombardment is also affected: ions experience sidewall collisions indeep strucures, and the bombardment at the bottom is reduced. These effects lead to a reduced etch rate indeep structures of high aspect ratio. RIE lag is not related to RIE reactors; it is presentin all plasma etching systems irrespective of actual reactor design



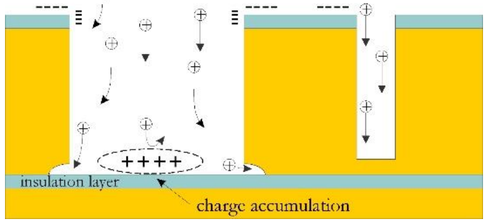
BOWING

Ion bowing is caused by the **diffraction of ions** while entering a trench/needle or by the negative potential of trench walls (needle wall) with respect to the plasma glow resulting in a deflection of these ions to the wall.

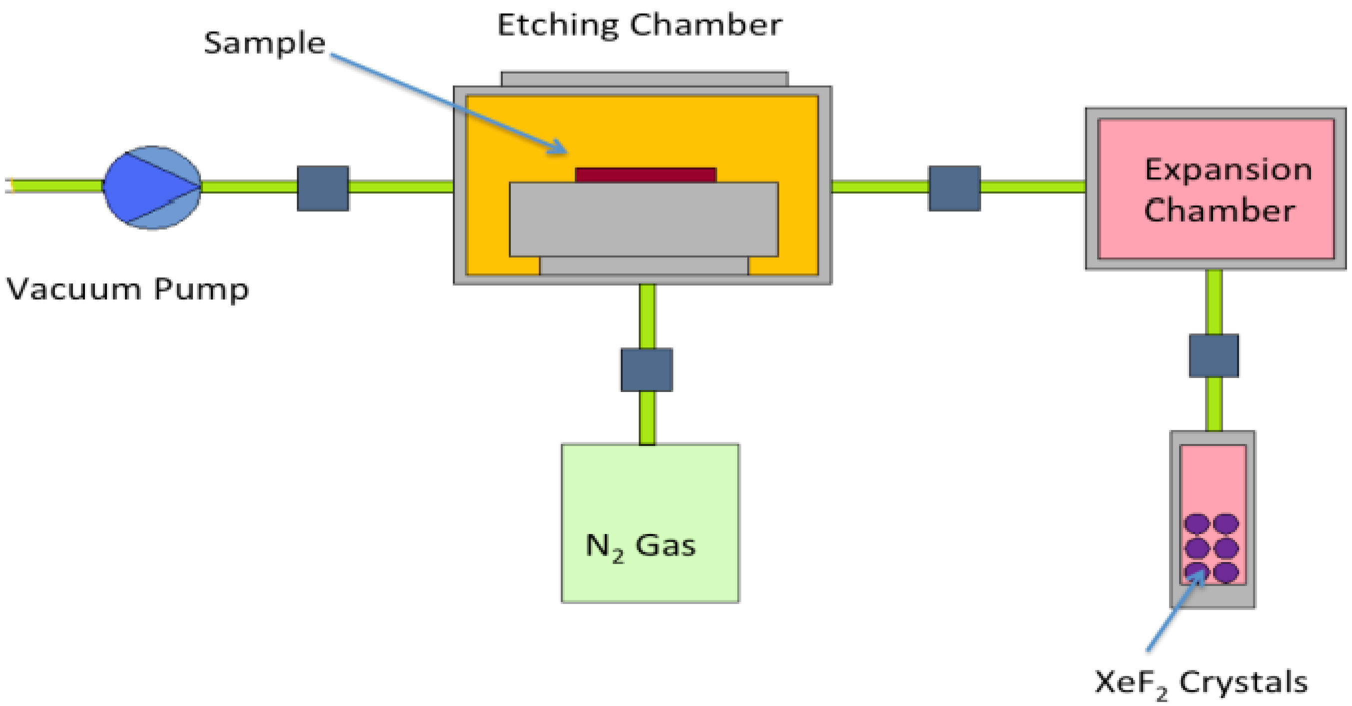


NOTCHING

When the silicon etching end point is reached, the underlying oxide (either oxide on the back side of a bulk wafer, or BOX) becomes charged. This charging leads to repellency of incoming ions, and they are deflected side ways, enhancing lateral etching near the silicon/oxide interface. Note that **RIE lag has an effect on notching**: the larger feature shave experienced longer overetching, therefore the notching effect has had more time to operate.

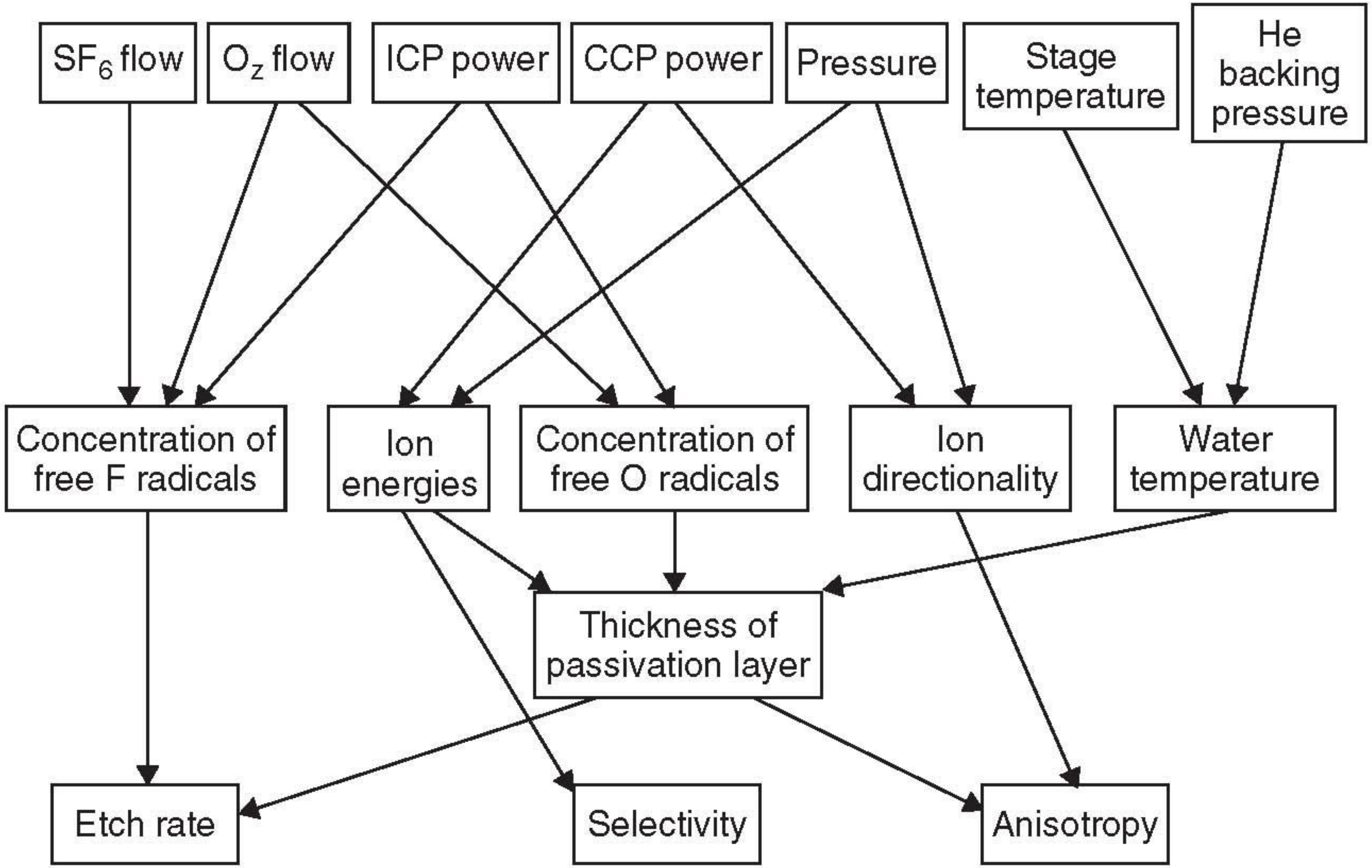


For the purpose of silicon etching, it is not even necessary to use a plasma source of fluorine radicals. A number of gaseous compounds are well known for the ability to etch silicon spontaneously, **without need for plasma excitation**. XeF_2 deliver fluorine radicals which once abdorbed onto the surface.



The reaction is exothermic and may result in an increase of temperature. This effect is mitigated by the use of **pulsed** rather than continuous etch system.

THE INTERDEPENDENCE OF REACTOR PARAMETERS TO PLASMA PARAMETERS AND ETCH RESPONSES ON A WAFER

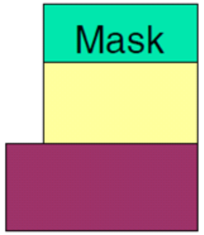


Profile → •**Isotropic** •**Anisotropic** •Mixed profile ⇐ **Undercut / Aspect ratio / Pattern density**

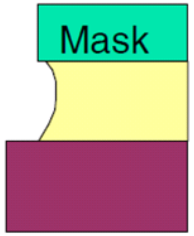
Selectivity → •**Flim/PR or Film/Mask** •**Film/Underlayer** ⇐ **CD Loss / Hard mask / Chemistry**

Uniformity → •**Across a wafer (Local)** •**Variations with feature size** •Wafer to wafer (Global) ⇐ **Macro-loading / Micro-loading / ARDE effect**

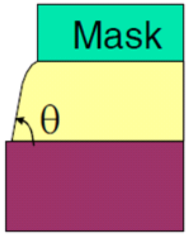
Surface quality → •**Contamination** •**Damage** •Texture ⇐ **Polymer Residue / Corrosion / Micro-trench & notch**



Anisotropic

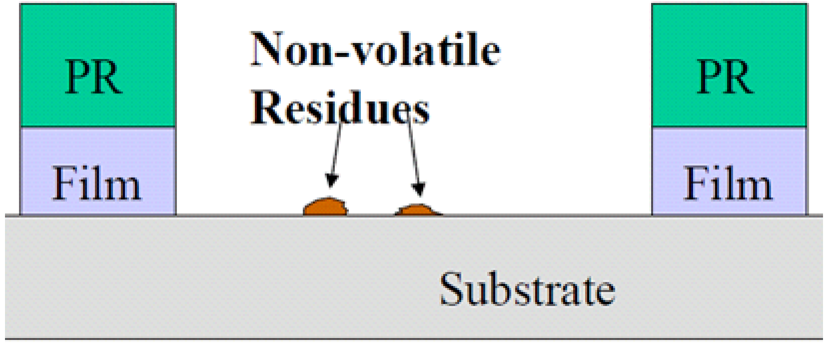


Bowed



Tapered or Sloped

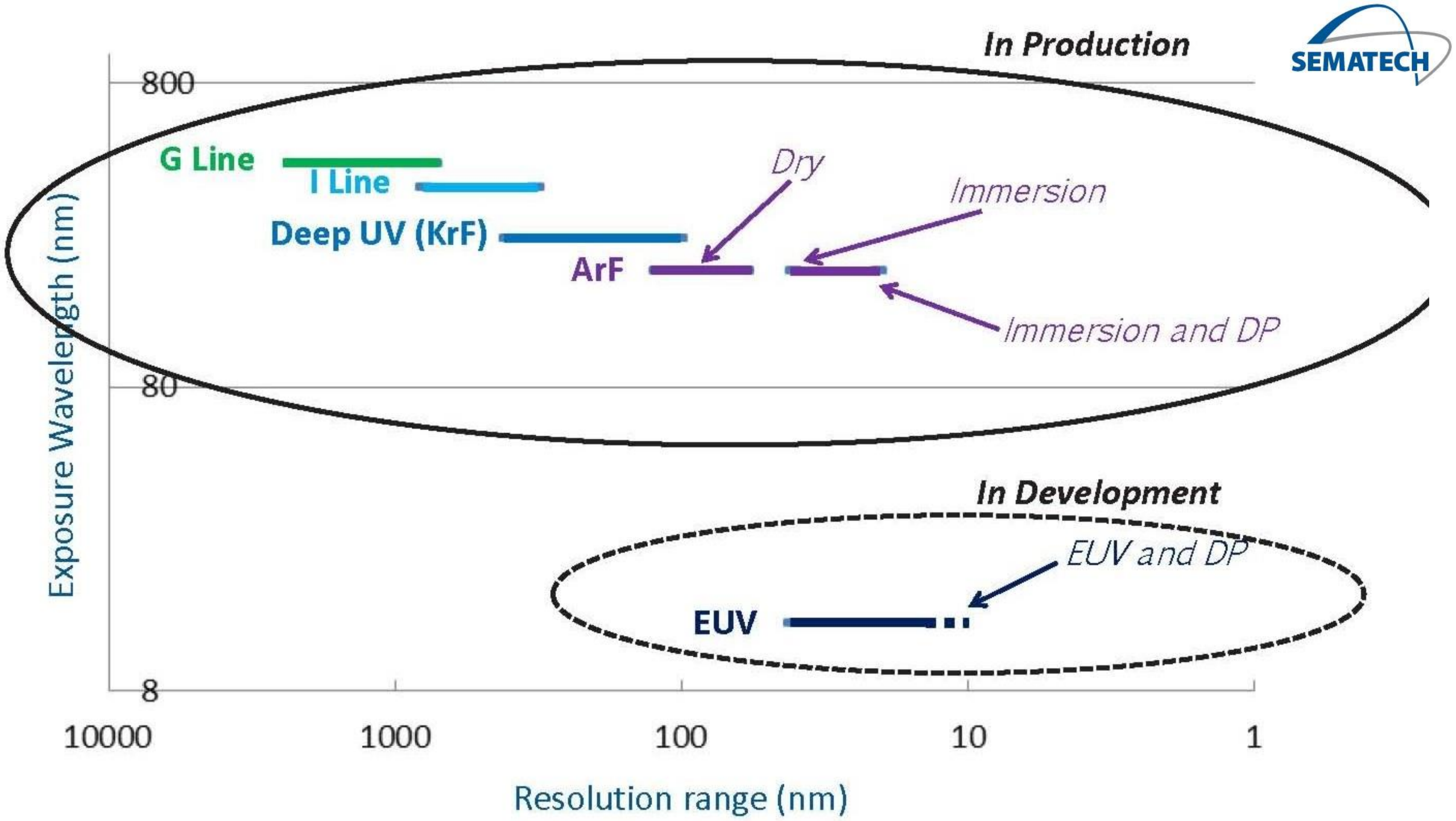
Etch profiles



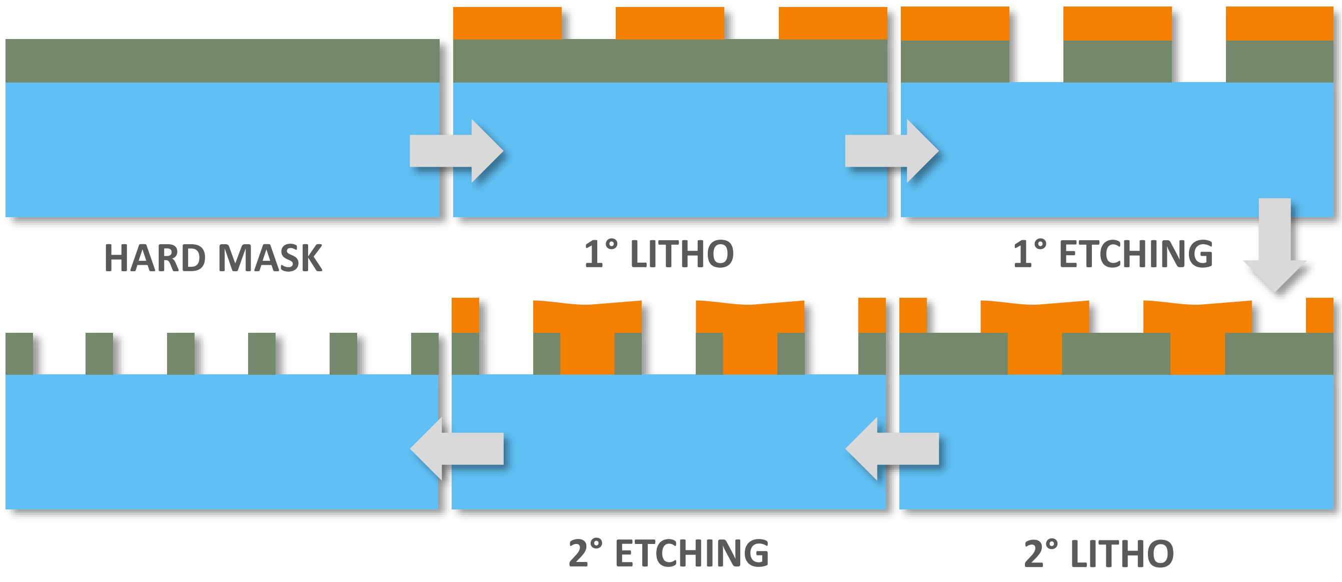
PR: photoresist
CD: critical dimension

TIPS & TRICKS

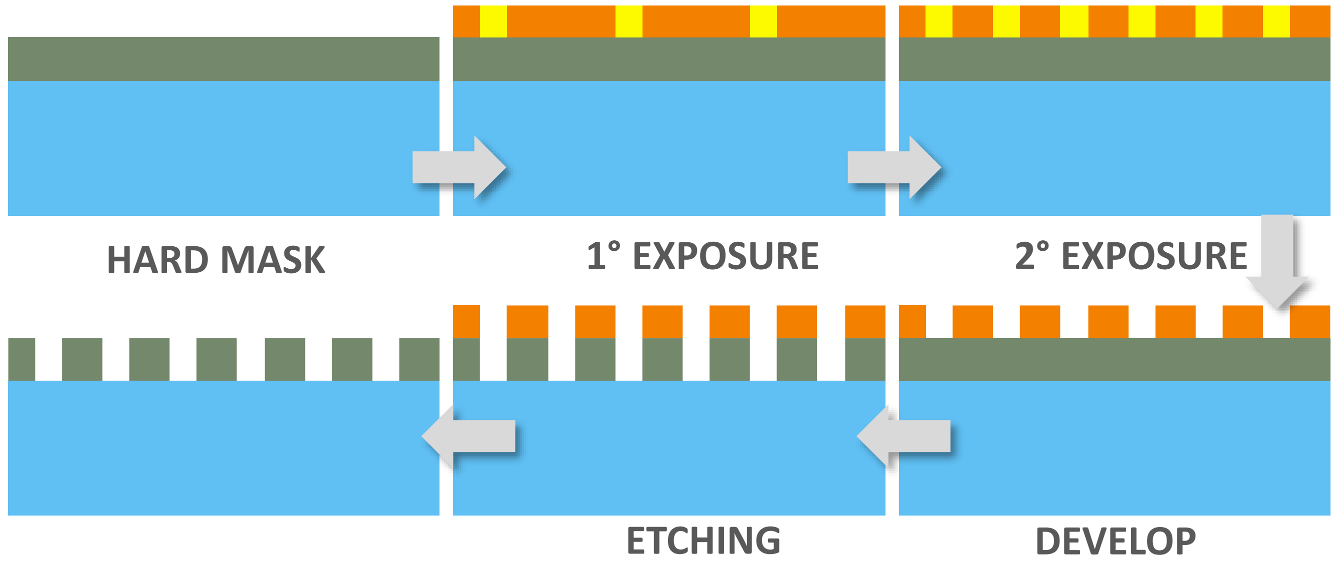
IMPROVEMENT THROUGH LITHO WAVELENGTH AND NA



DOUBLE PATTERNING

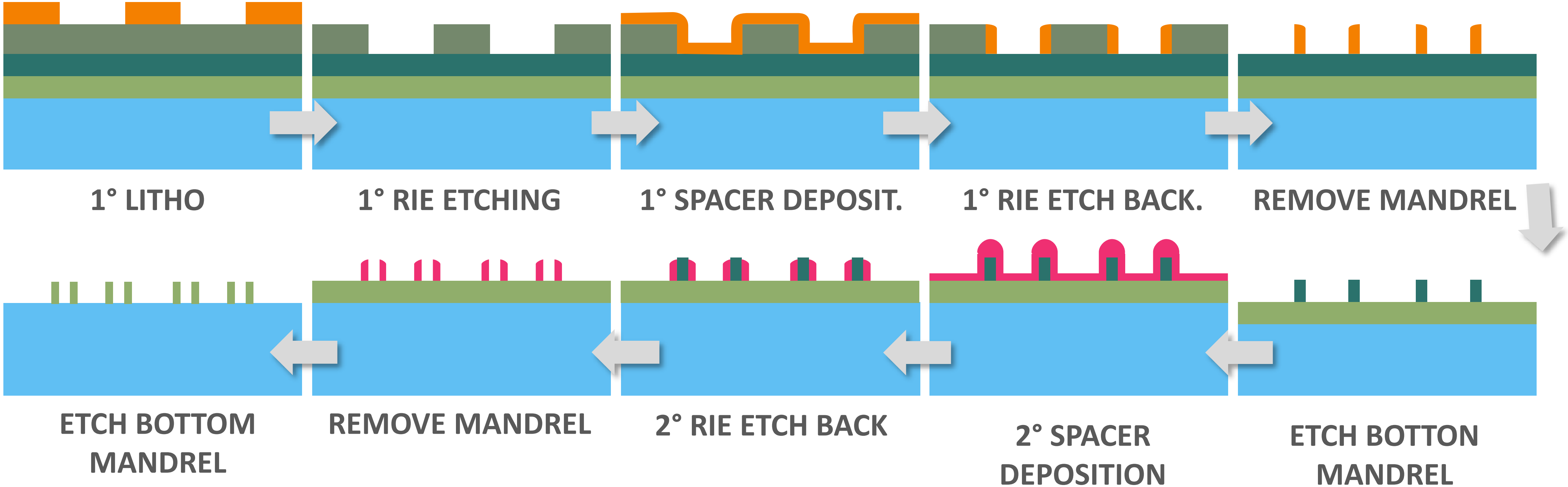


DOUBLE EXPOSURES



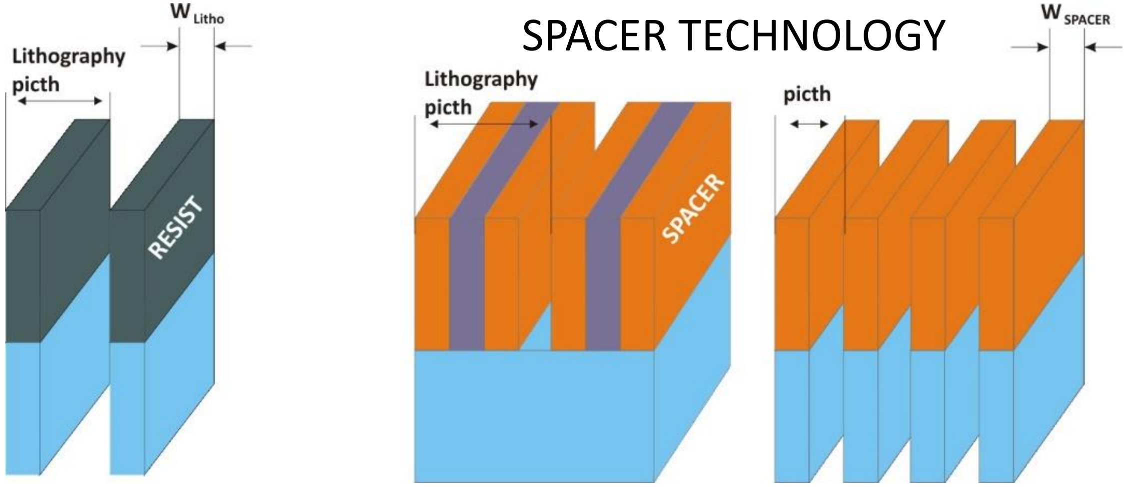
SELF ALIGNED DOUBLE PATTERNING TEHCNIQUE

Self Aligned Double Patterning (SADP) -- Pitch multiplication by process

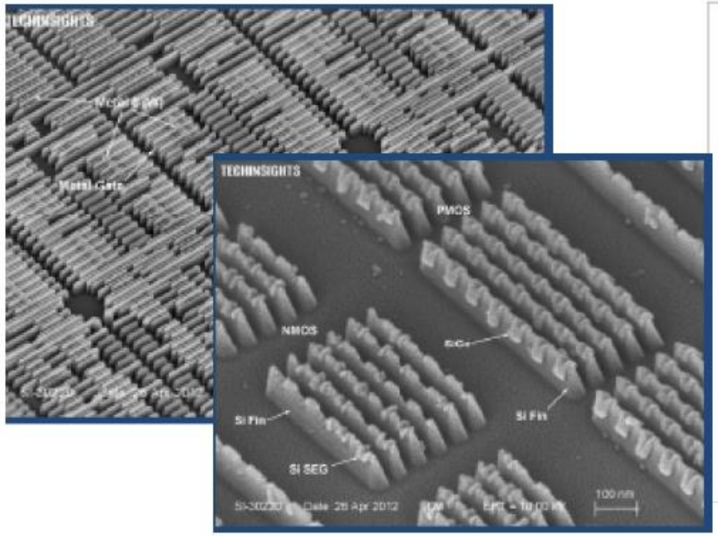


STANDARD LITHOGRAPHY

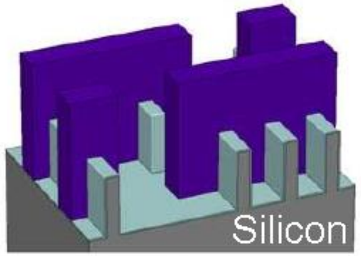
SPACER TECHNOLOGY



FinFET Formation – Scalable to 10nm w/o EUV

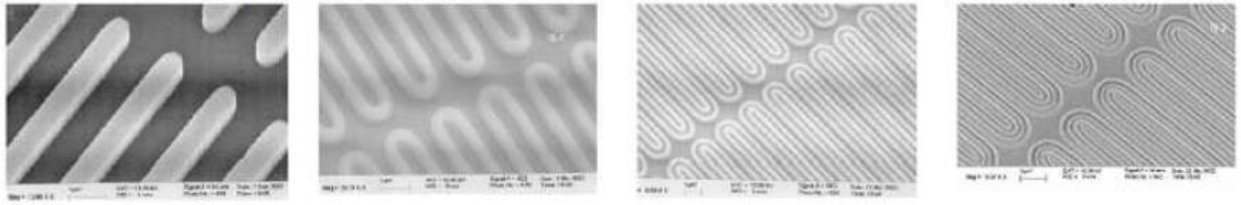


Self Aligned Double Patterning
With Cut Mask for Fin and Gate



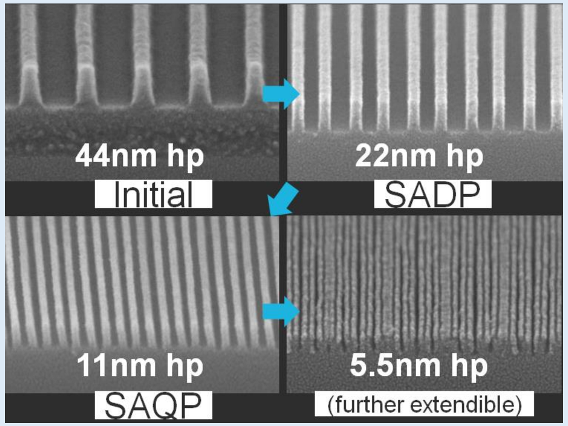
*TechInsights, Intel Ivybridge

Photo-lithographically defined sacrificial structures | 1st Spacers | 2nd Spacers | 3rd Spacers



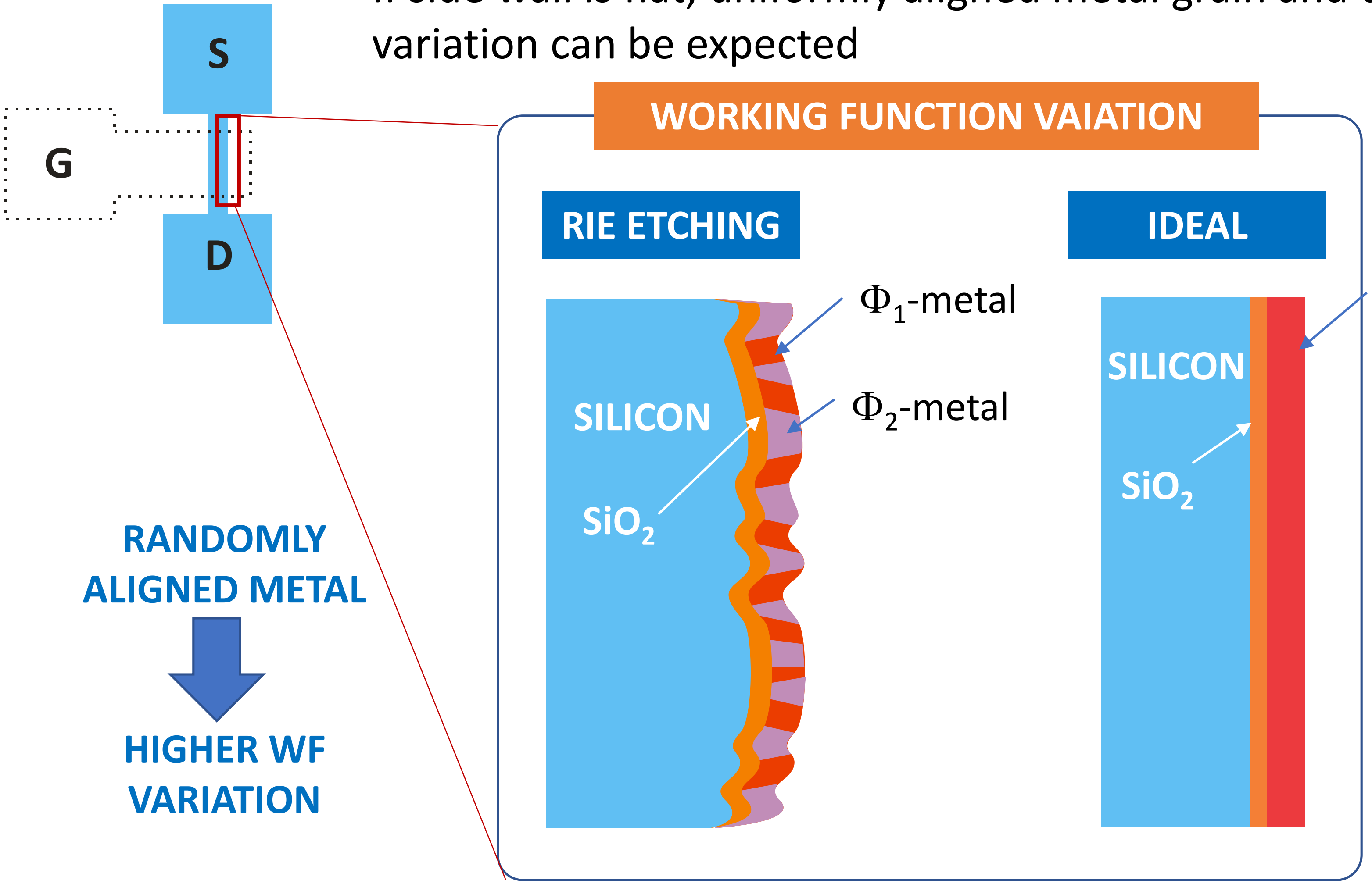
By Applied Materials

SELF-ALIGNED MULTIPLE PATTERNING



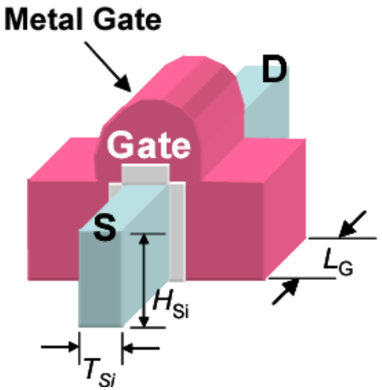
By TOKIO Electron

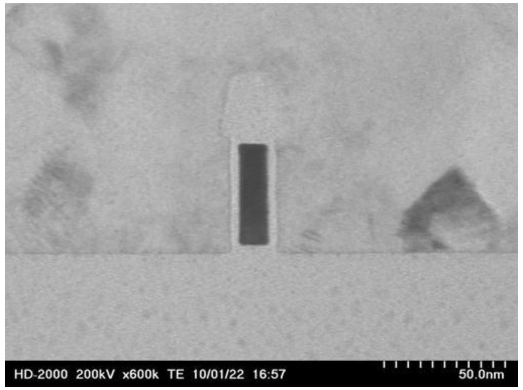
Rough etched side wall causes randomly aligned metal grain and thus higher WF variation
If side wall is flat, uniformly aligned metal grain and thus lower WF variation can be expected

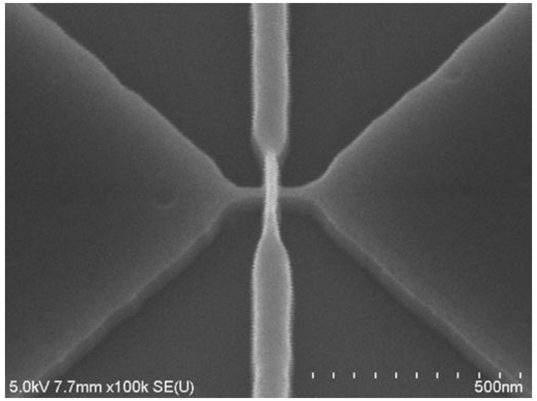


RANDOMLY ALIGNED METAL → HIGHER WF VARIATION

UNIFORMLY ALIGNED METAL → LOWER WF VARIATION



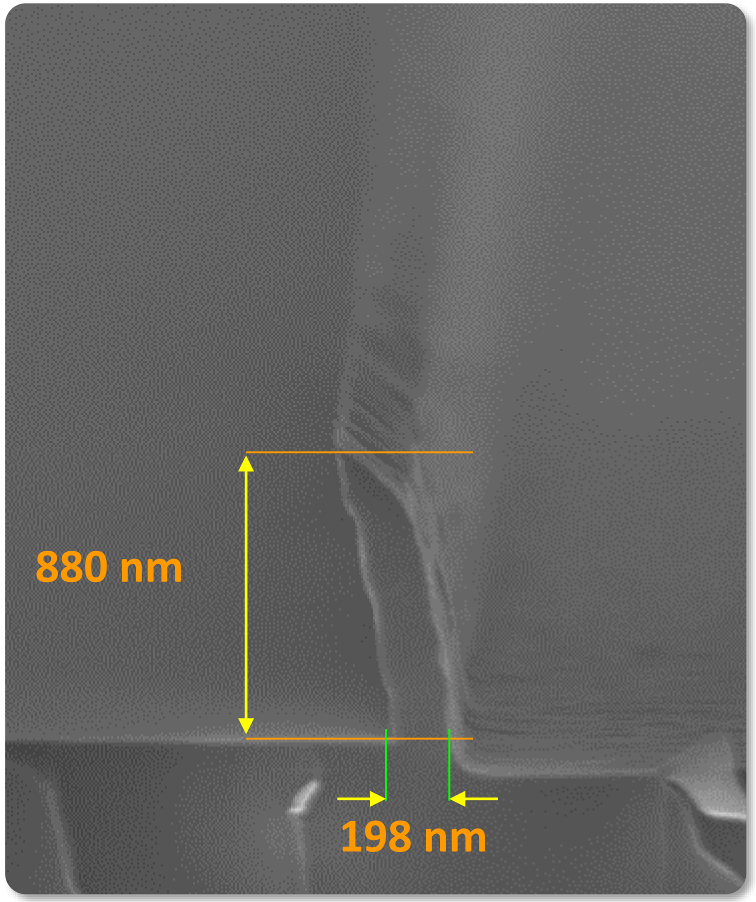




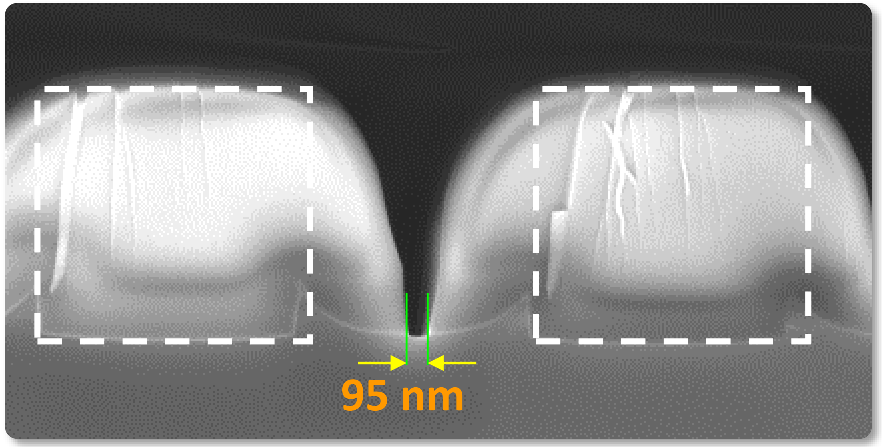
MICROFABRICATION OF THE NANOMETRIC STRUCTURES

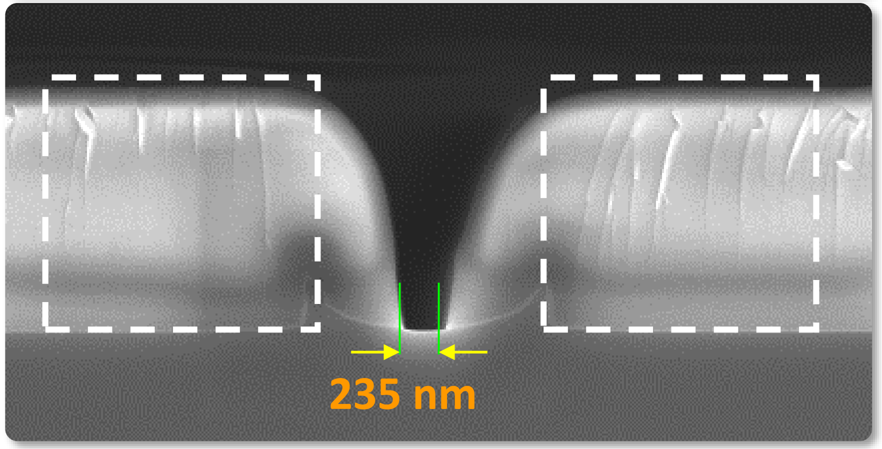
- **Standard CMOS process**: near-UV lithography, chemical vapor deposition (CVD), reactive ion etching (RIE)...
- **Spacer techniques** allowed for the definition of submicron features and gaps of the coupling structures
- Features down to **300 nm with conventional micrometric lithography**

EXAMPLE OF SILICON NANOLINE



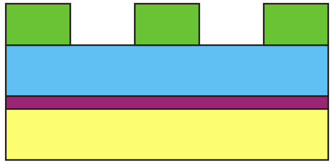
EXAMPLES OF NANO-GAP



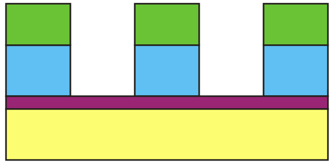


Si_3N_4 LPCVD DEPOSITION

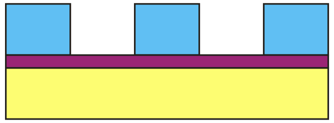
SiO_2 LPCVD DEPOSITION



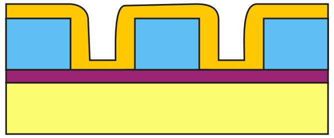
SiO_2 PATTERNING



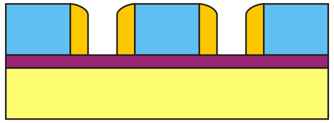
SiO_2 RIE ETCHING



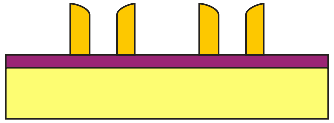
PHOTORESIST ETCHING



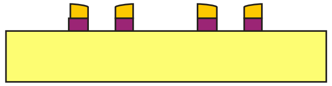
DEPOSITION CONFORMAL LAYER



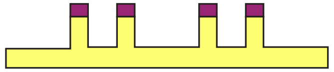
RIE MASKLESS (ETCHBACK)



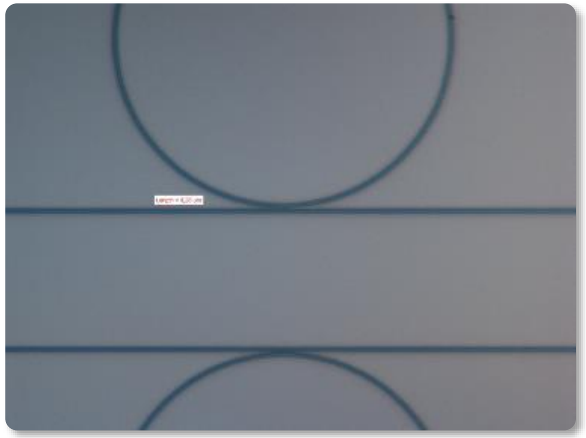
SiO_2 WET ETCHING

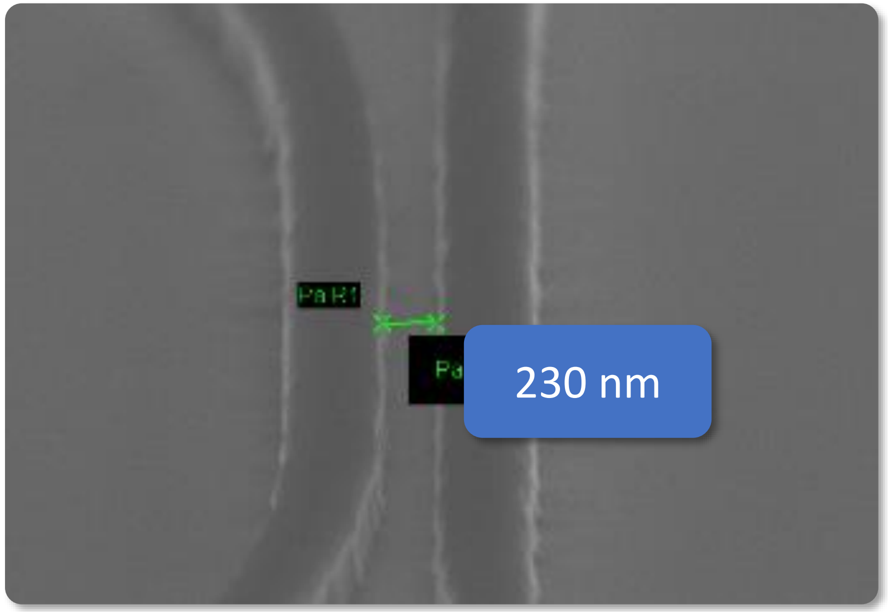


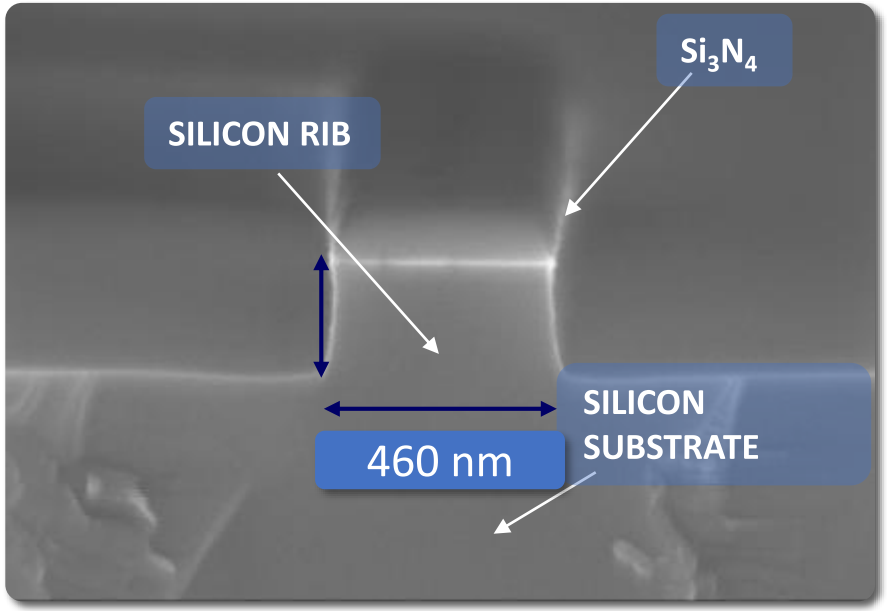
Si_3N_4 RIE ETCHING

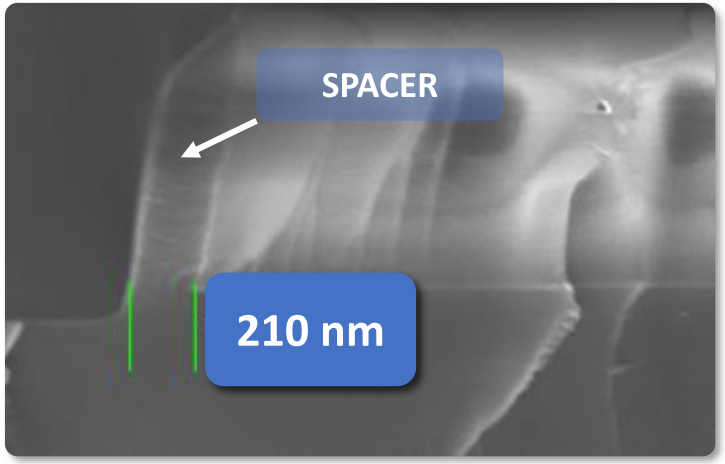


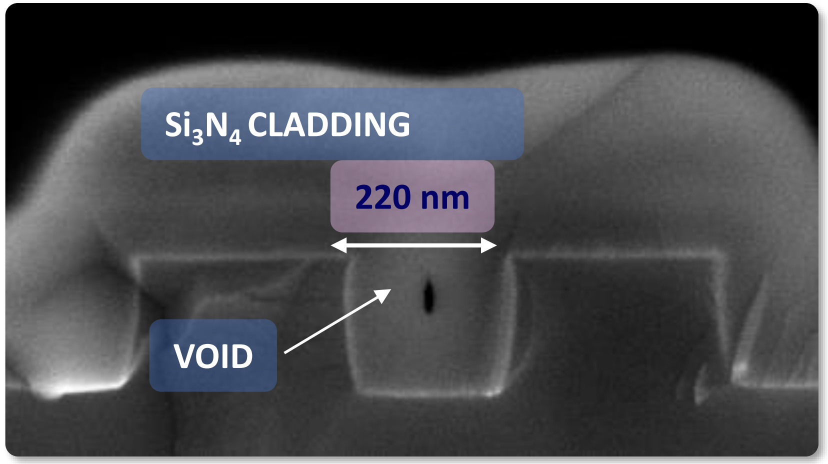
SILICON RIE ETCHING

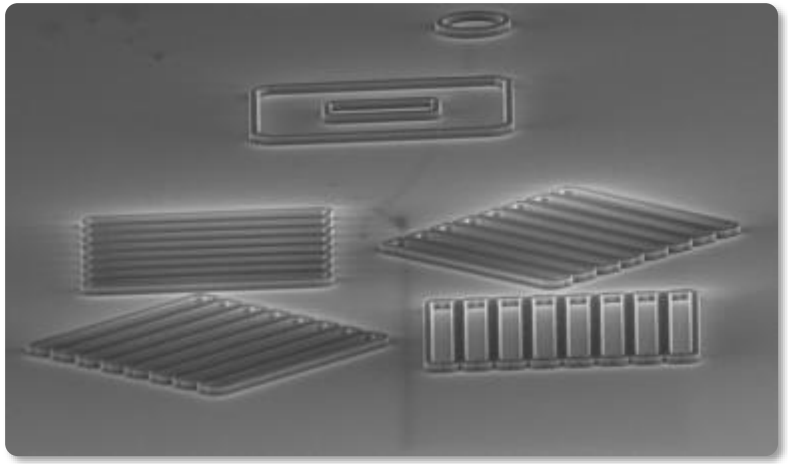



230 nm

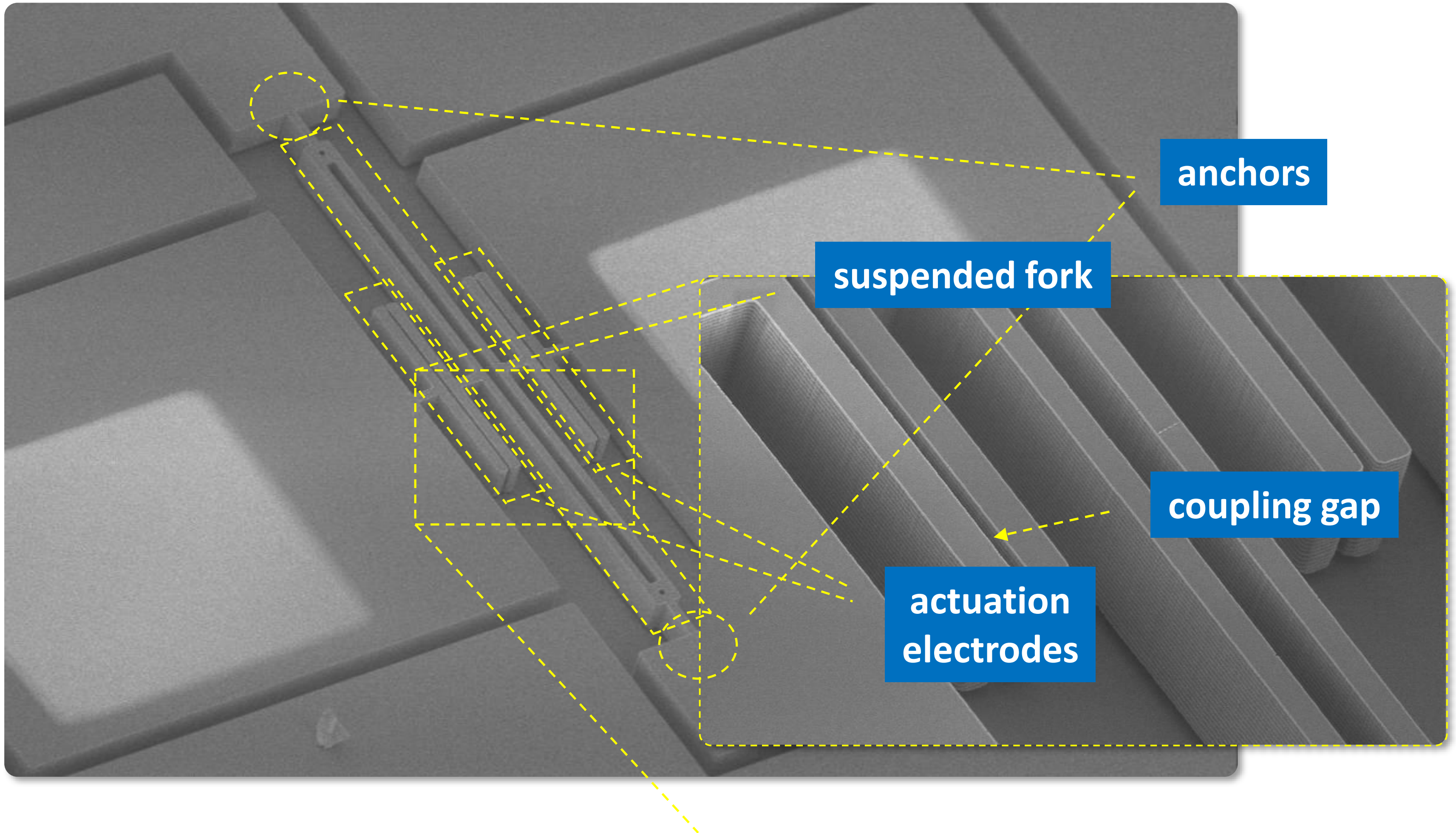

Si_3N_4
SILICON RIB
460 nm
SILICON SUBSTRATE

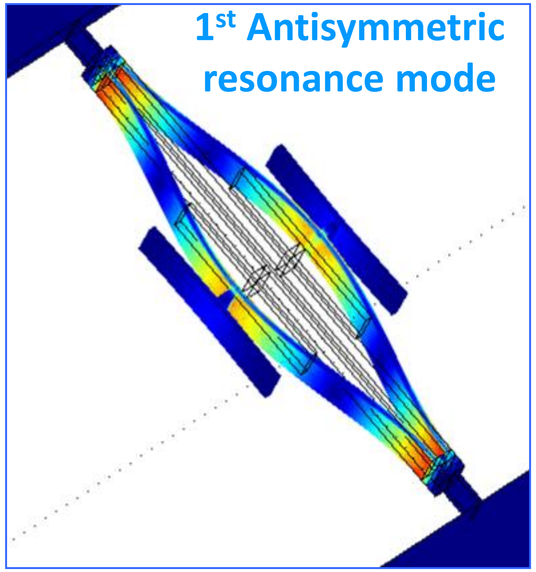

SPACER
210 nm

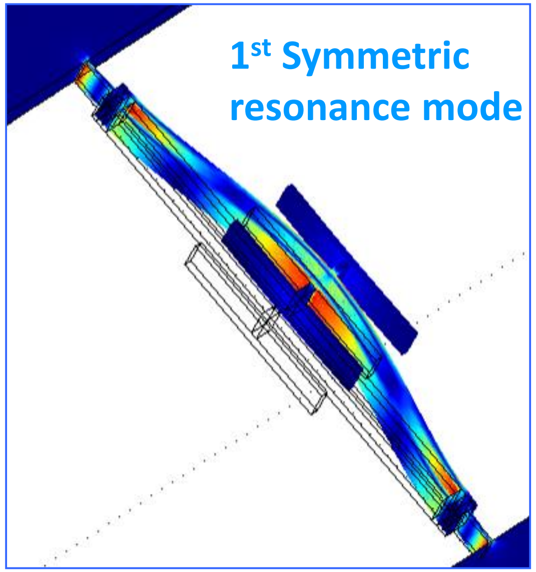

Si_3N_4 CLADDING
220 nm
VOID



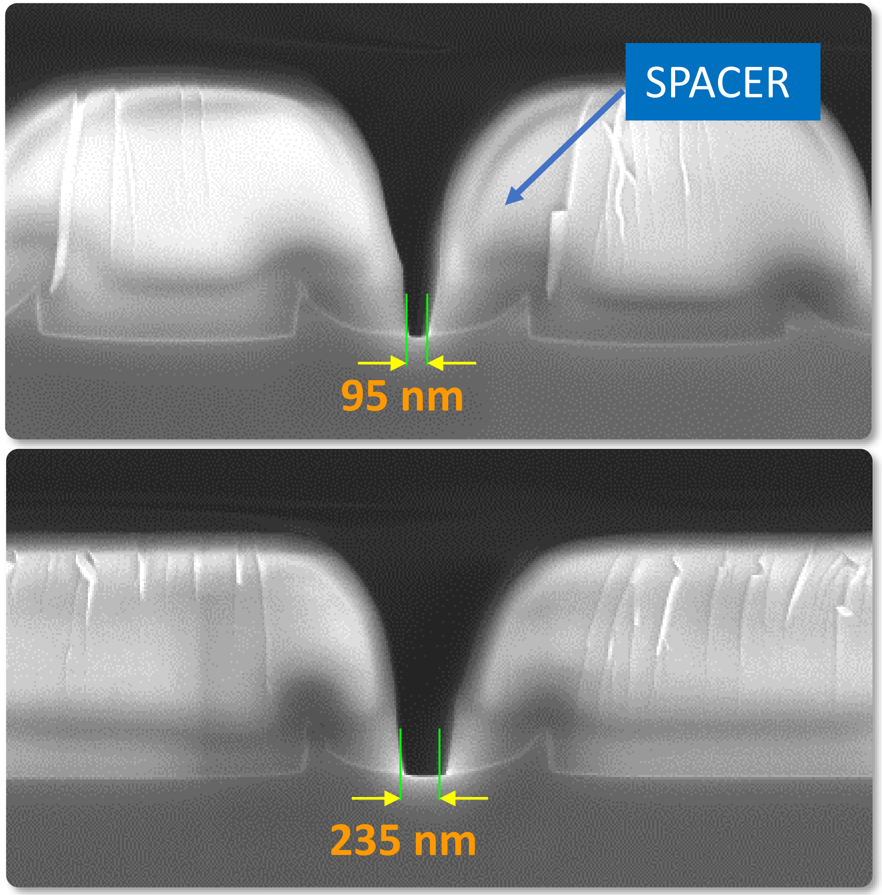
RESONANT MEMS STRAIN SENSORS

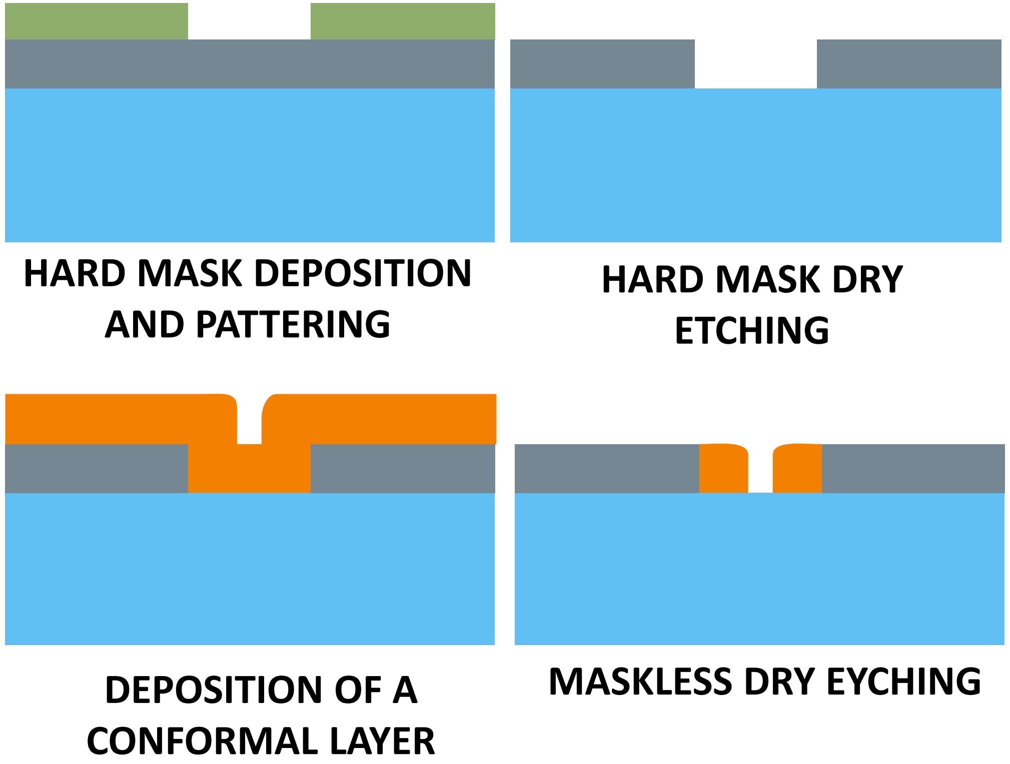

anchors
suspended fork
coupling gap
actuation electrodes


1st Antisymmetric resonance mode


1st Symmetric resonance mode

EXAMPLES OF NANO-GAP



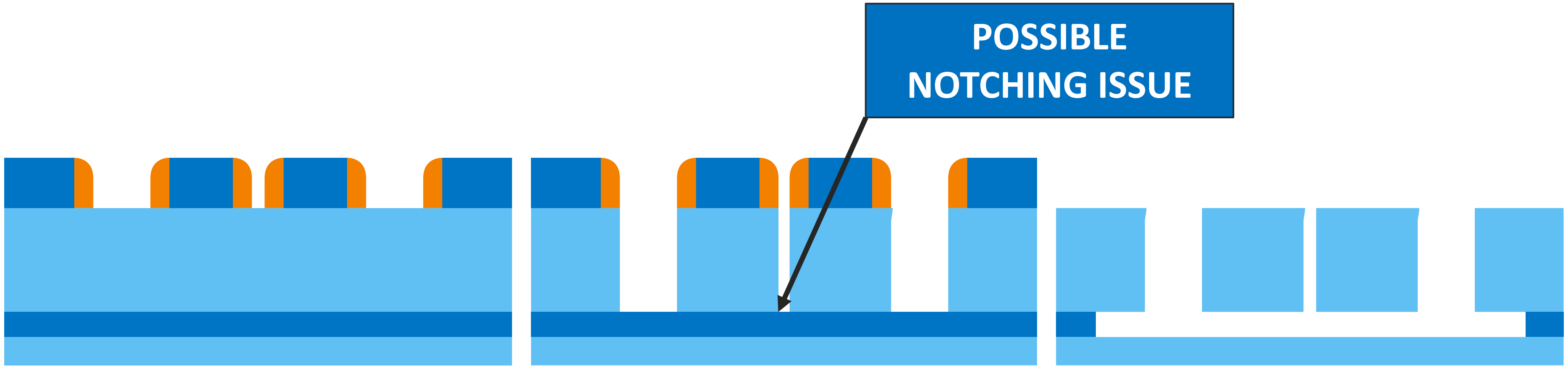


Silion-On-Insulator (SOI) TECHNOLOGIES

HARD AMSK DEPOSITION AND PATTERNING

HARD MASK DRY EYCHING

DEPOSITION OF A CONFORMAL LAYER

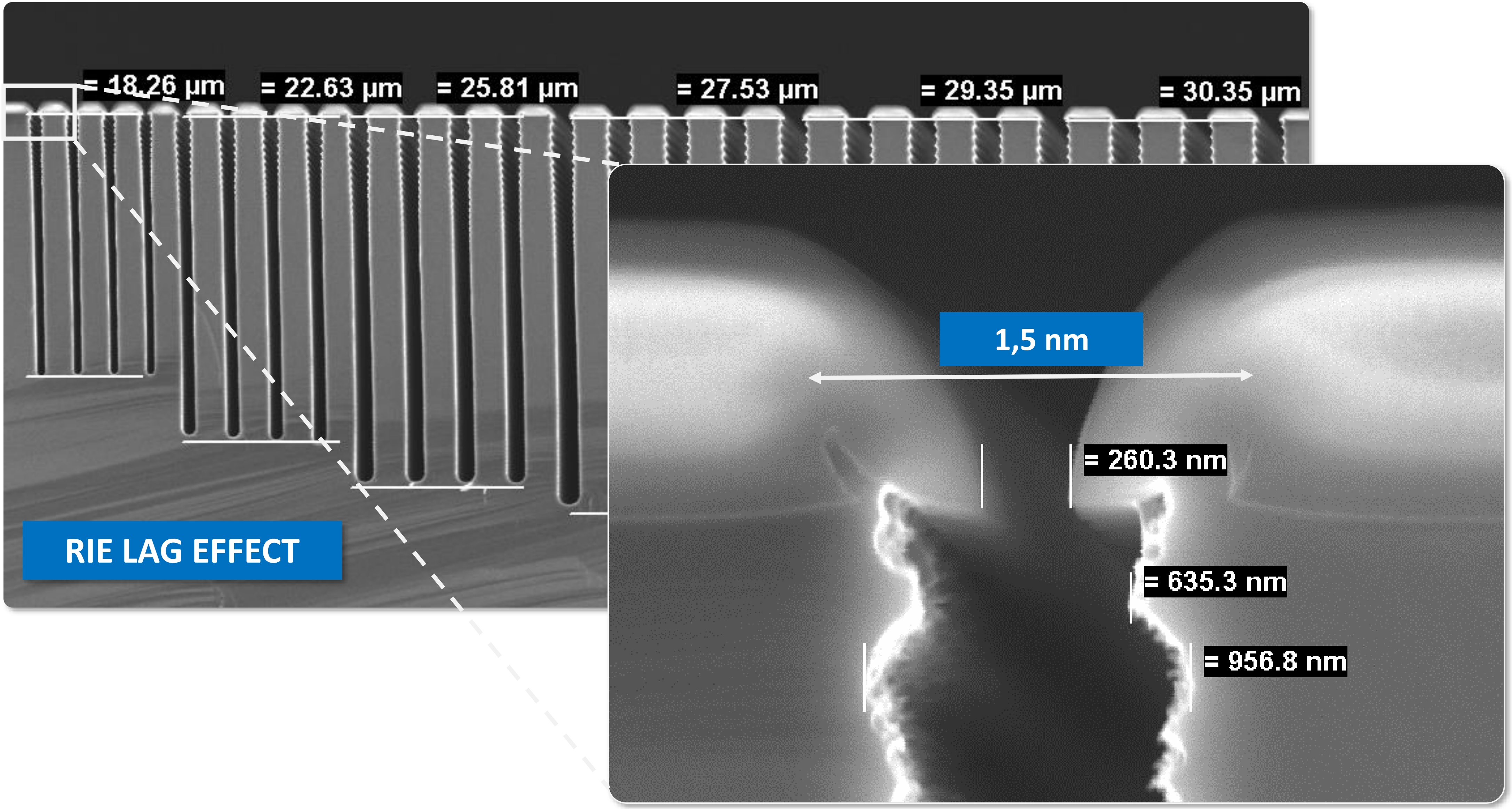


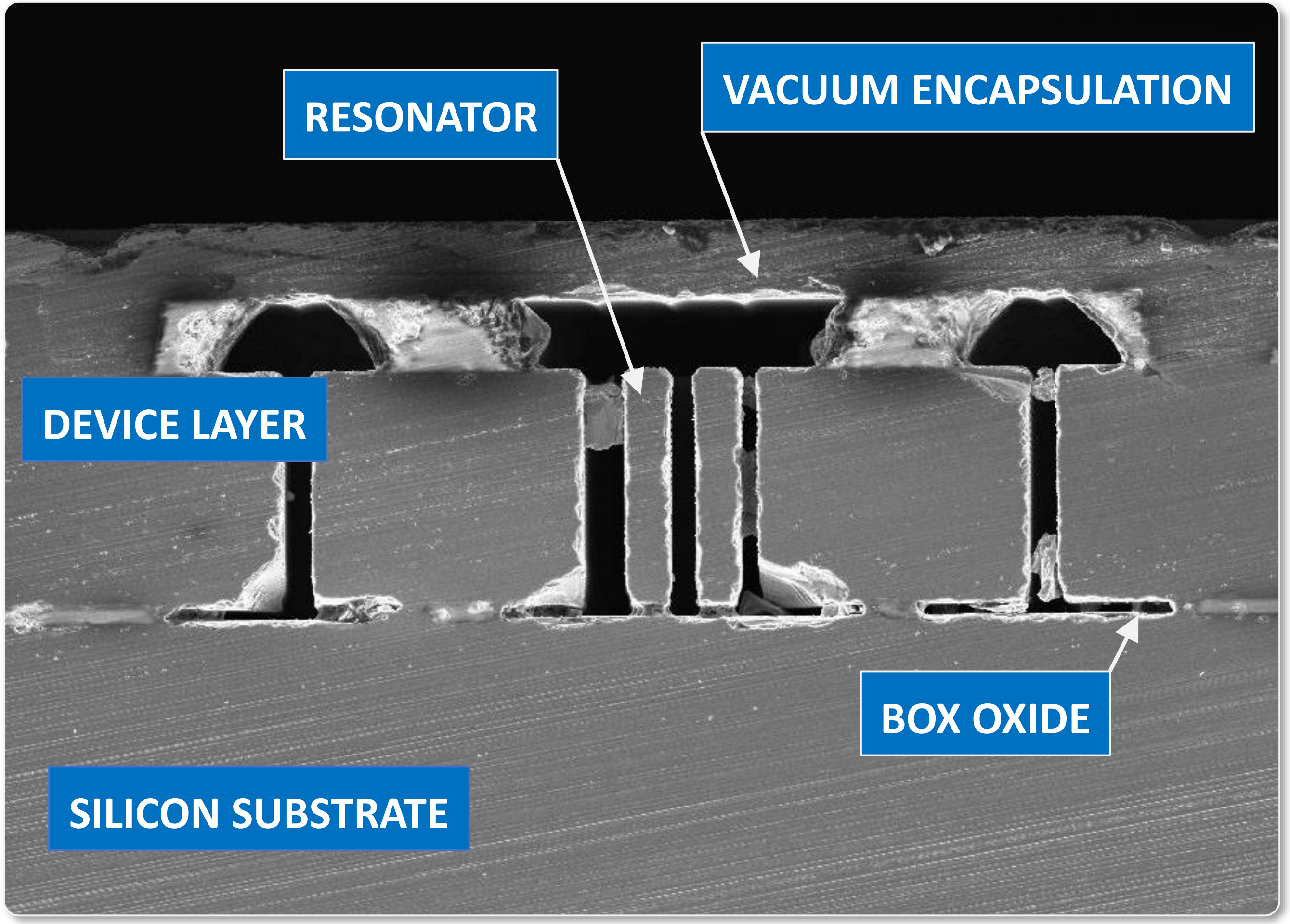
MASKLESS DRY ETCHING

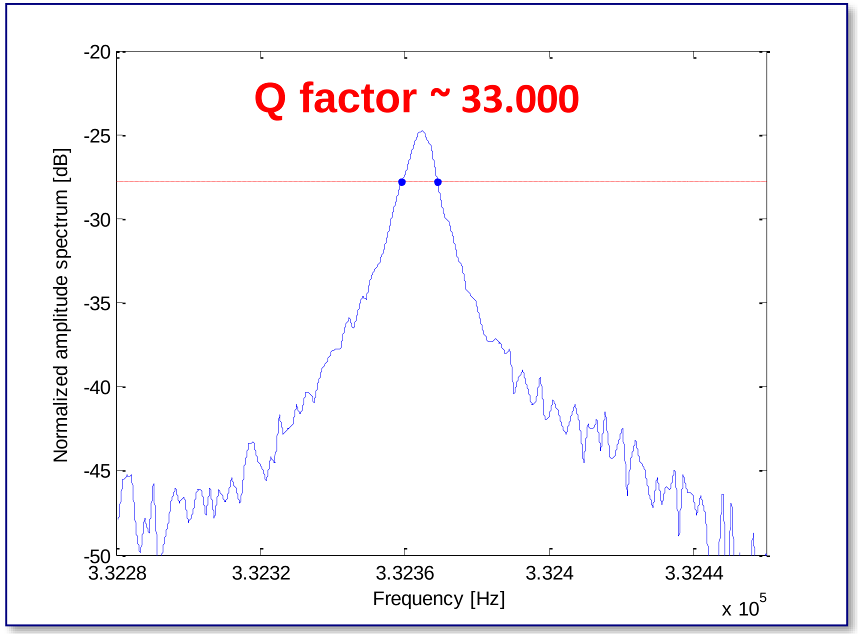
DEEP RIE SILICON DEVICE LAYER ETCHING

SiO_2 ETCHING – RELEASE OF THE DEFT STRUCTURE

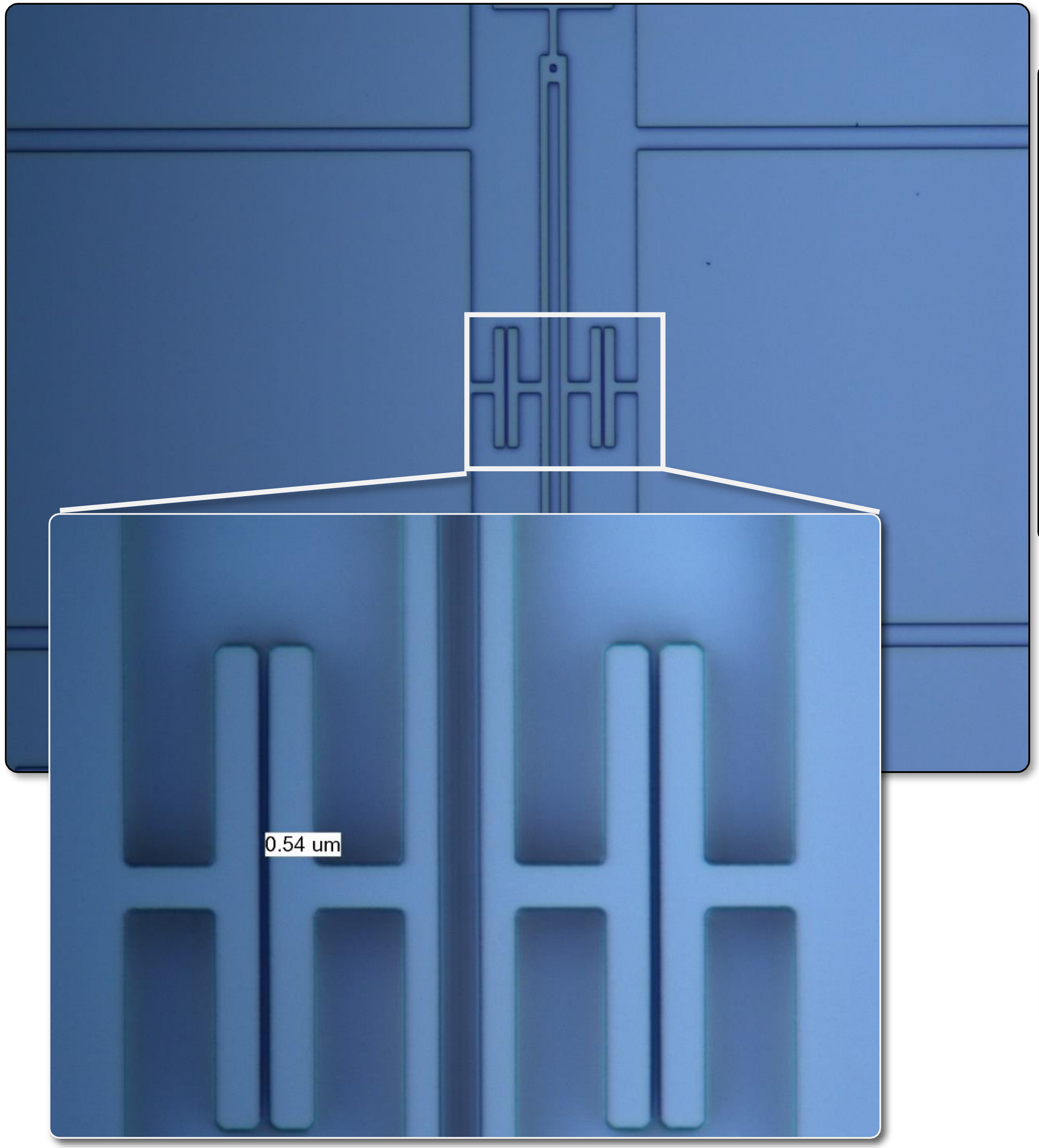
DEEP RIE SILICON DEVICE LAYER ETCHING

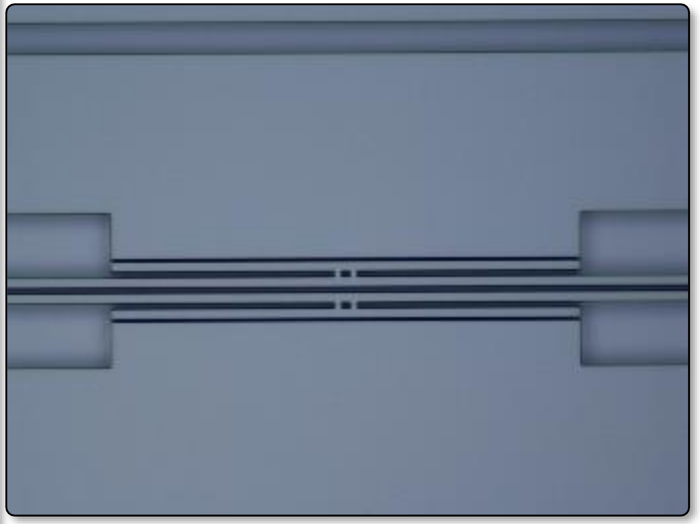


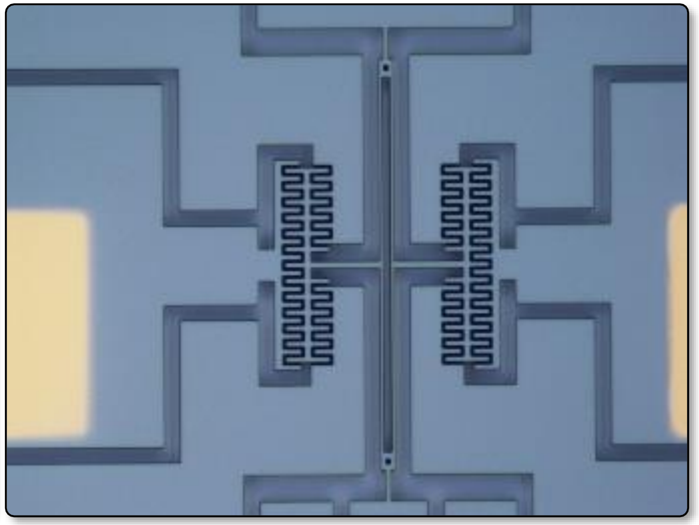

RESONATOR
VACUUM ENCAPSULATION
DEVICE LAYER
BOX OXIDE
SILICON SUBSTRATE

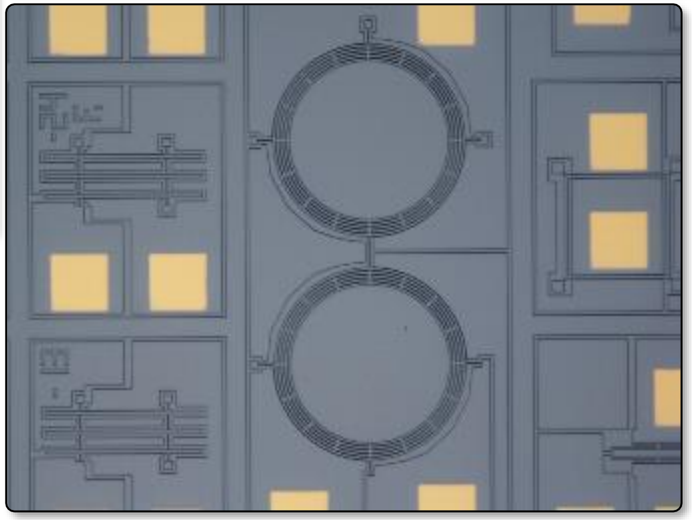

Q factor ~ 33.000
-20
-25
-30
-35
-40
-45
-50
Normalized amplitude spectrum [dB]
3.3228
3.3232
3.3236
3.324
3.3244
Frequency [Hz]
x 10^5

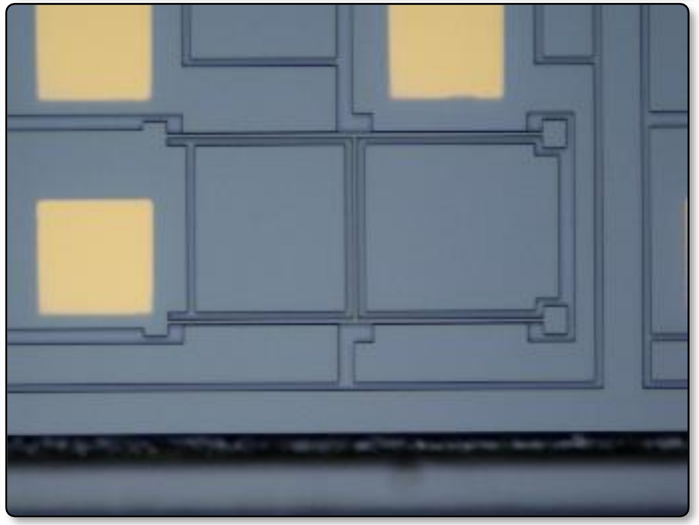
MEMS FABRICATION: RESONATORS WITH VARIOUS GEOMETRIES





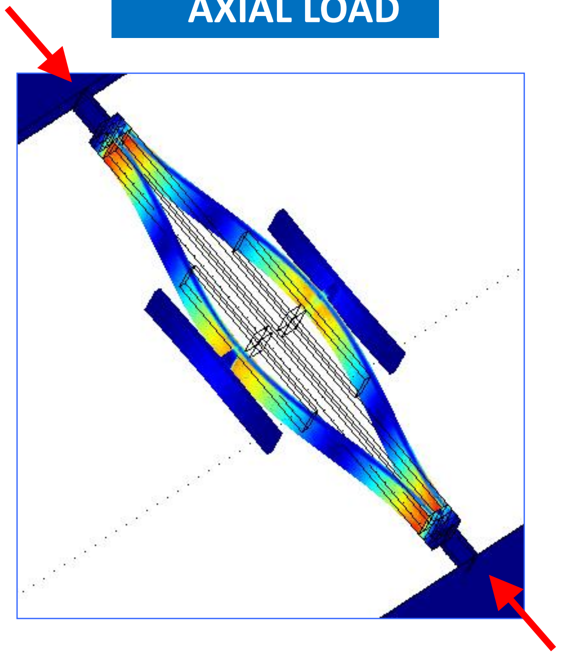




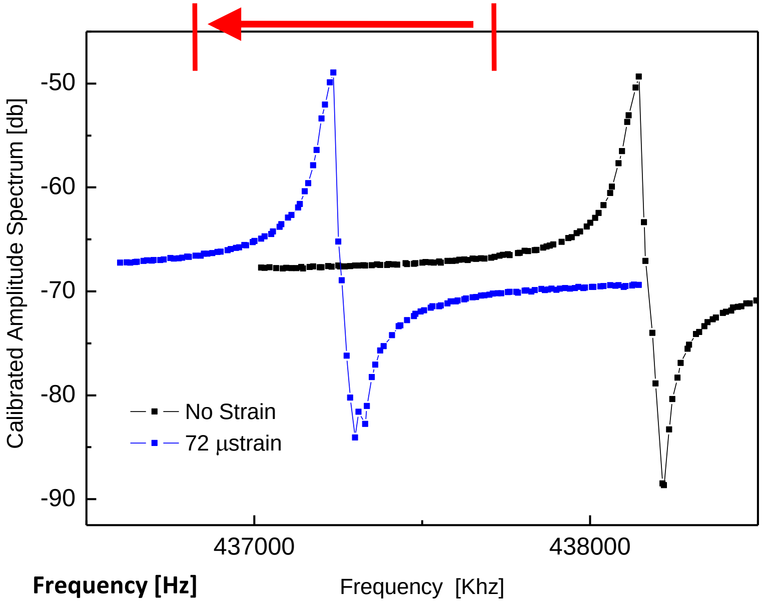


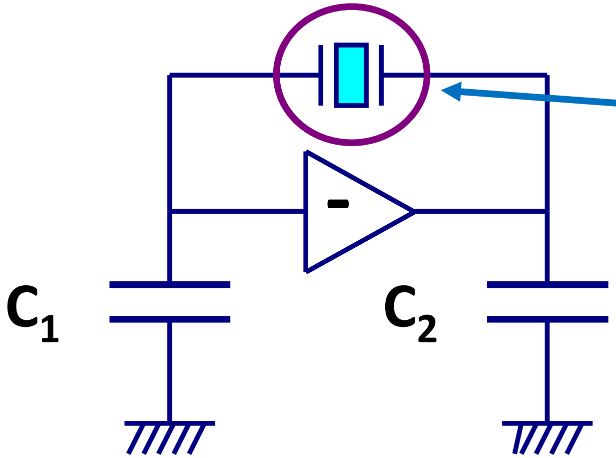
MEMS RESONATORS AS STRAIN SENSORS

AXIAL LOAD



RESONANCE FREQUENCY SHIFT





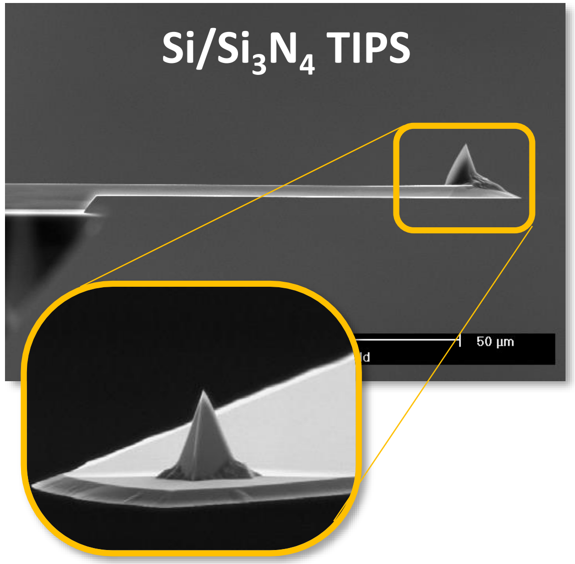
MEMS

SELF-SUSTAINED OSCILLATION AT RESONANCE

STRAIN-DEPENDENT OSCILLATOR

COMBINATION OF ISOTROPIC/ANISOTROPIC SILICON DRY ETCHING FOR MICROFLUIDIC APPLICATIONS

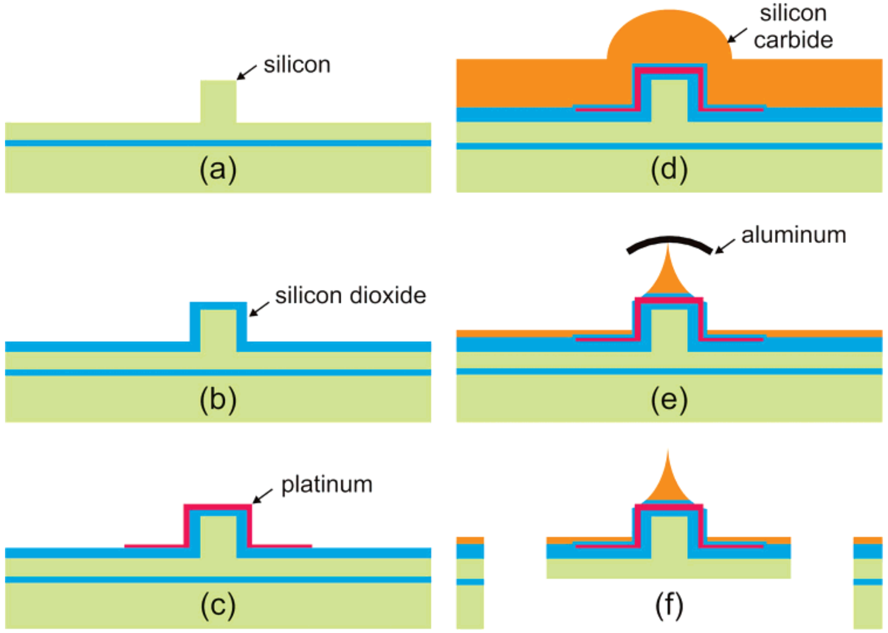
ATOMIC FORCE MICROSCOPE TIPS



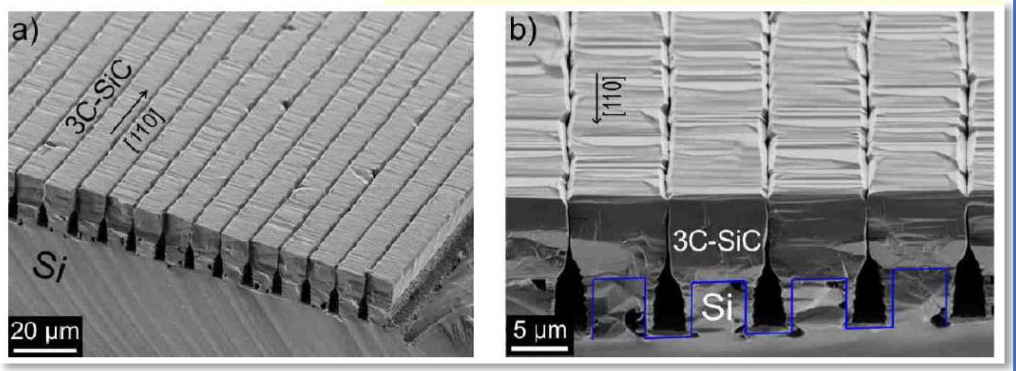
Anisotropic wet etching of silicon by KOH

REFERENCE:
Oliver Krause - NanoWorld Services GmbH

PECVD SiC

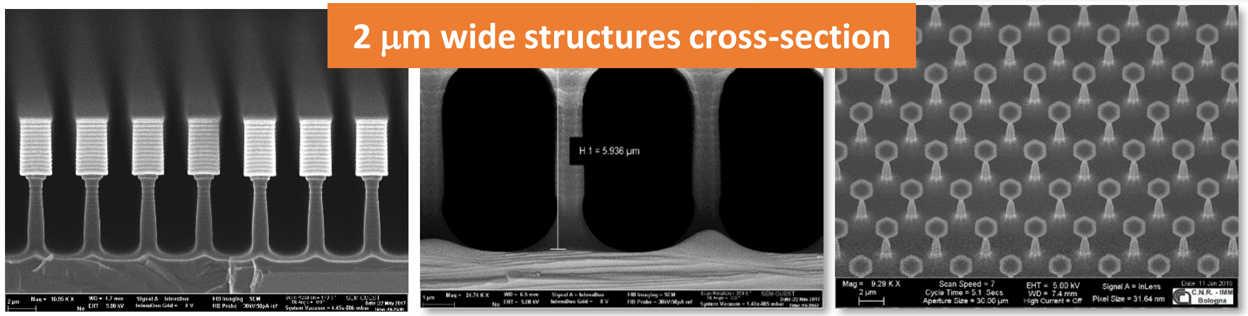


Jeyavel Velmurugan, Amit Agrawal, Sangmin An, Eric Choudhary, and Veronika A. Szalai; **"Batch Fabrication of Atomic Force Microscopy Probes with Recessed Integrated Ring Microelectrodes at a Wafer Level";** Anal. Chem. 2007, 79, 4769-4777

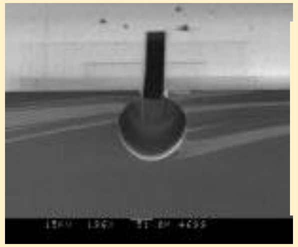


Toolbox of solutions for the reduction of defects in bulk cubic silicon carbide material
Proposed a new approach to improve the quality and to reduce stress modifying the structure of the substrate (compliance substrate) in order to force the system to reduce the defects while increasing the thickness of the layer

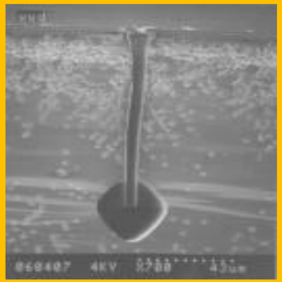
2 µm wide structures cross-section



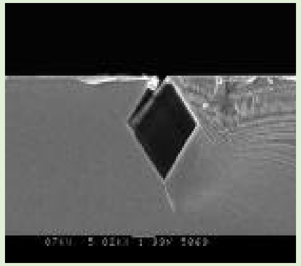
«CHALLENGE» H2020 EUROPEN PROJECT
3C-Si etero-epitaxilly grown on silicon compliance substrates and new 3C-SiC substrates for sustainable wide-band-gap power devices
www.h2020challenge.ue



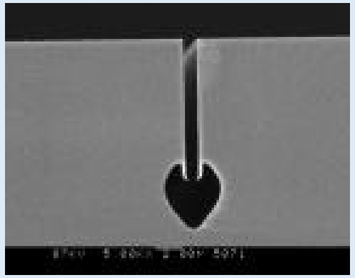
Circular channel etched electrochemically in an 5% aqueous HF solution



Circular channel obtained after wet chemical etching in HF-HNO_3 solution



V-groove channel obtained after KOH etching



Pear-shaped channel, obtained by isotropic RIE

«***Micromachining of buried micro channels in silicon***»,
De Boer, M.J.aEmail Author, Tjerkstra, R.W.b, Berenschot, J.W.a, Jansen, H.V.c, Burger, G.J.d, Gardeniers, J.G.E.a, Elwenspoek, M.a, Van Den Berg, Journal of Microelectromechanical Systems, Volume 9, Issue 1, March 2000, Pages 94-103

The gas-chromatographic separation principle:
Based on specific affinity between sample and "stationary phase"

IDLE AND SAMPLING

INJECTION

SEPARATION

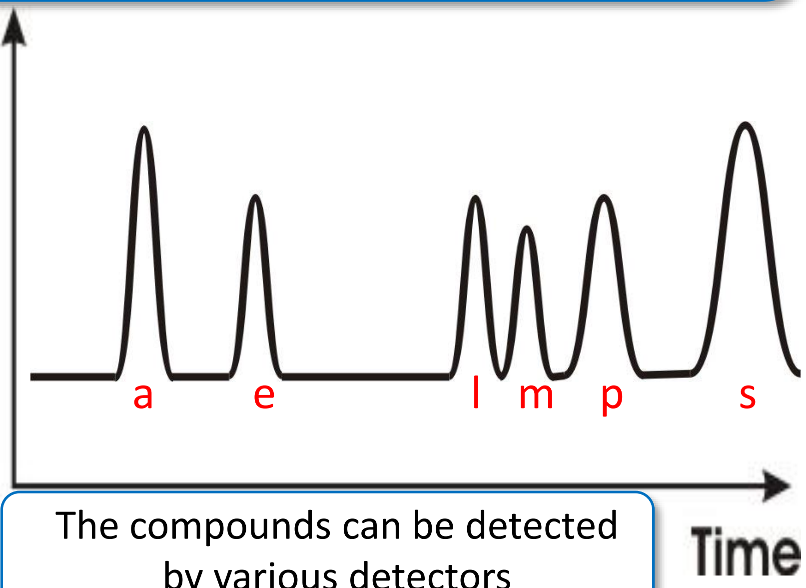
a
m
p
l
e

The compounds are separated on the column by how they interact with these phases; gas is the mobile phase.
The Peak area is proporzional to element concentration

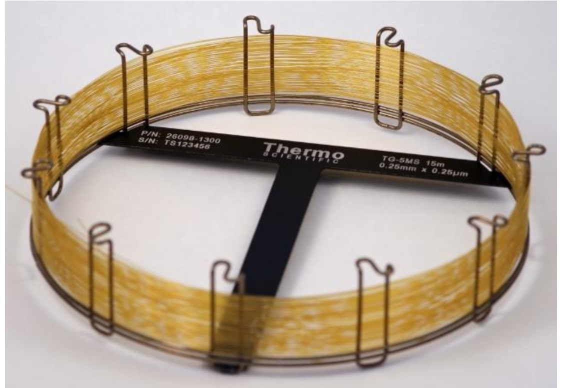
Carrier gas ⇒⇒

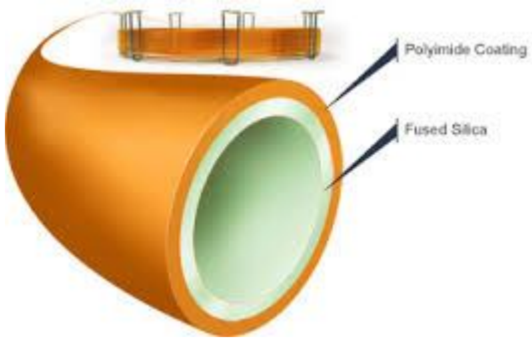
Compounds are injected onto the GC column

The inner sidewall of a column is covered by a stationary phase

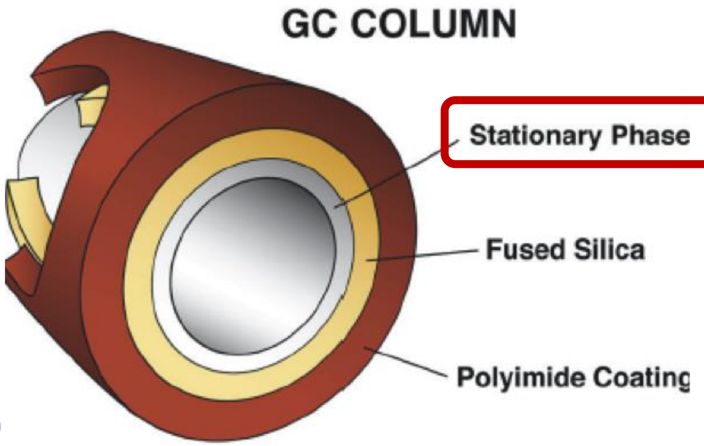


The compounds can be detected by various detectors





STANDARD FUSED SILICA COLUMN FOR GAS CHROMATOGRAPHY



1

The uniformity of the steady-phase thickness is one of the constraints for achieving better separation and resolution

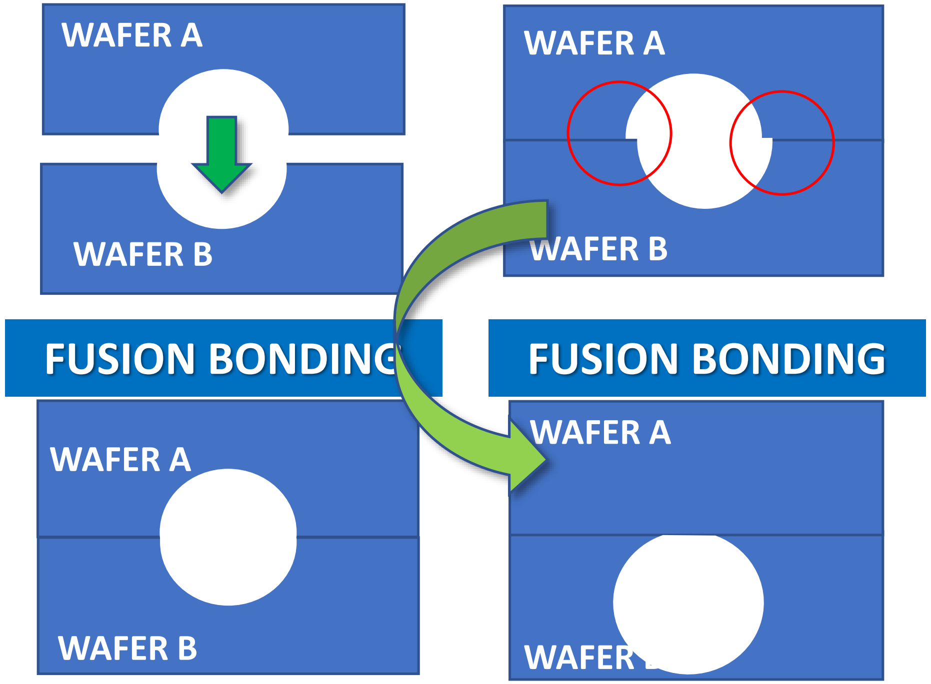
2

FAST-GC: guarantee fast analysis cycles, minimal dead volumes, low costs and high portability for in-field use.

DEVELOPING AND MANUFACTURING OF A MEMS BASED CIRCULAR GC COLUMN FOR FAST-GC

COMBINATION OF ISOTROPIC/ANISOTROPIC SILICON DRY ETCHING

SILICON CHANNELS WITH CIRCULAR CROSS-SECTION

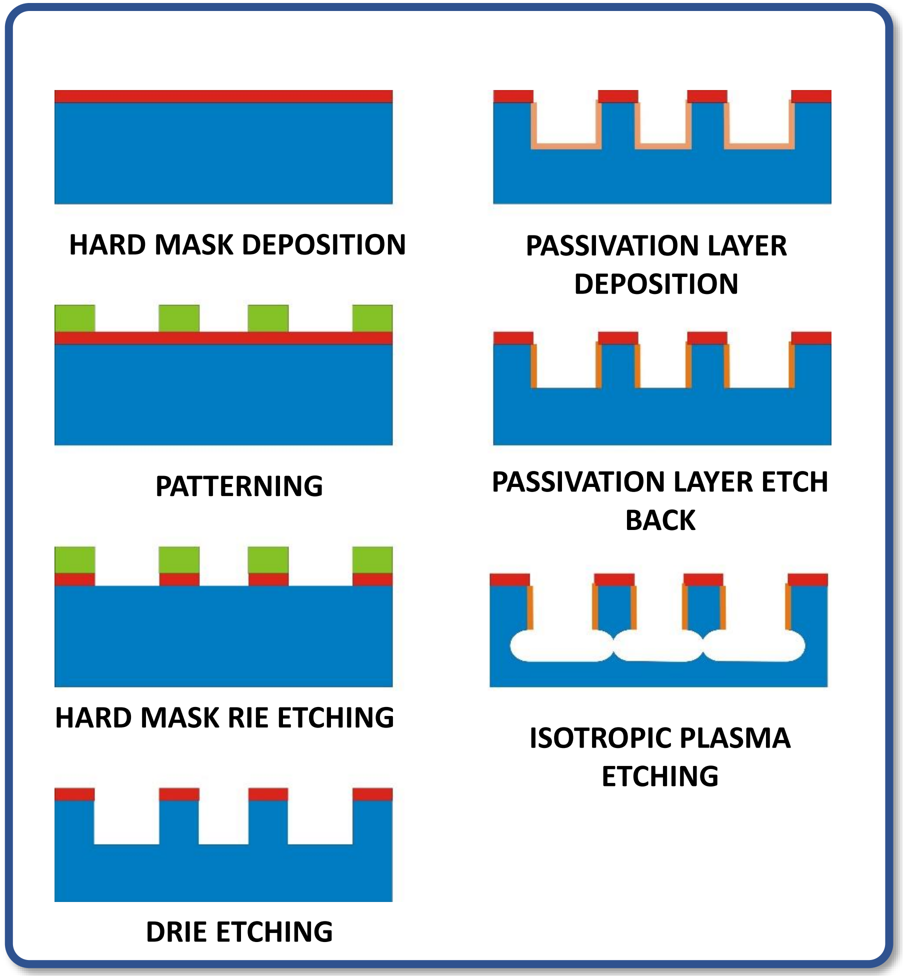


SCREAM PROCESS

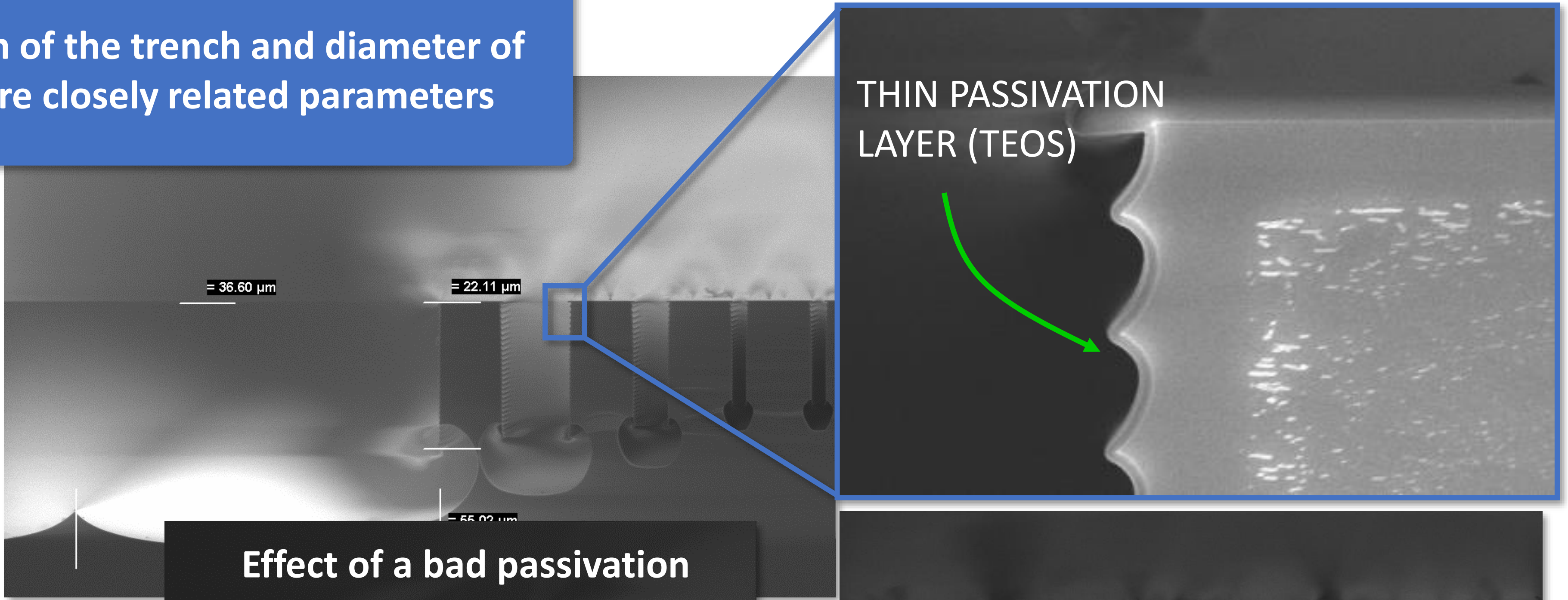
- ✓ First demonstrated by MacDonald’s group at Cornell University
- ✓ Single crystal silicon (SCS) microstructures
- ✓ Post-CMOS process for electronics integration

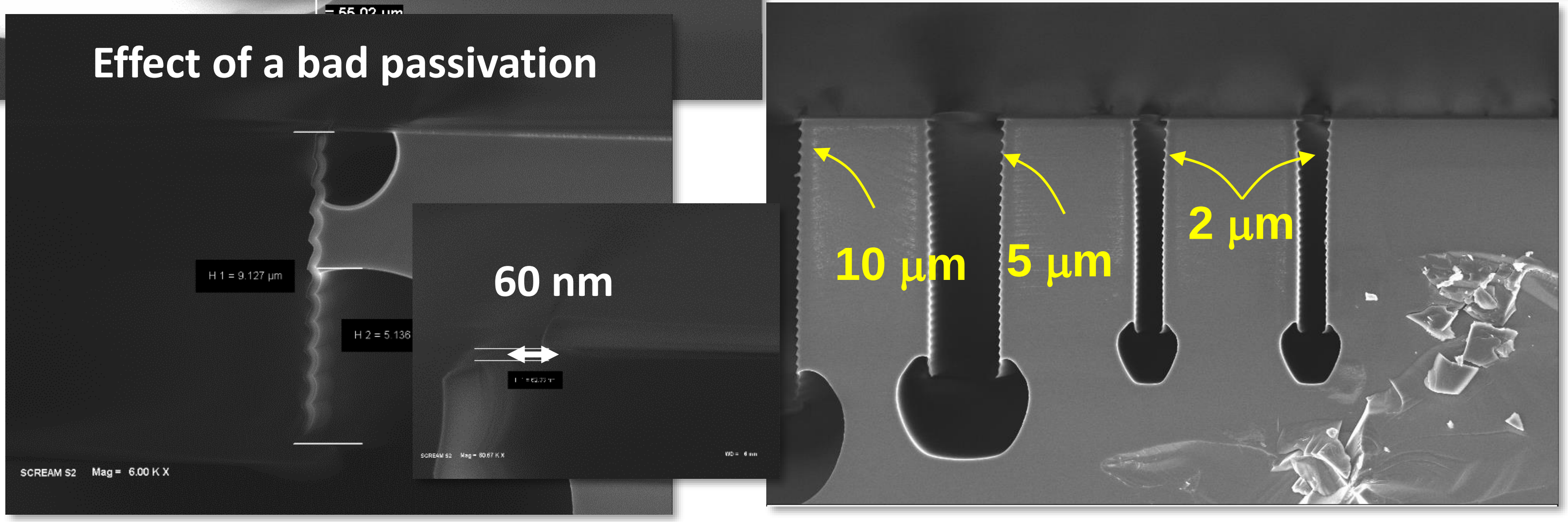
TRENCH SIDEWALL PASSIVATION LAYER

- THERMAL SILICON OXIDATION
- LPCVD CONFORMAL THIN LAYER
- PLASMA POLYMERIZED FLUOROCARBON THIN (USING PASSIVATION STEP OF A BOSCH PROCESS CYCLE)
- PARYLENE THIN LAYER

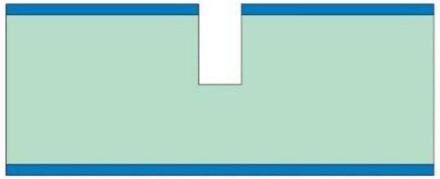


Width, depth of the trench and diameter of the bubble are closely related parameters

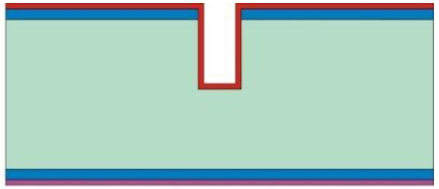




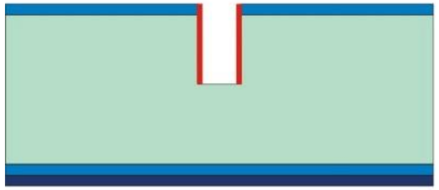
HARD MASK DEPOSITION



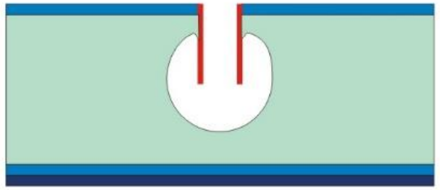
TRENCHS by D-RIE



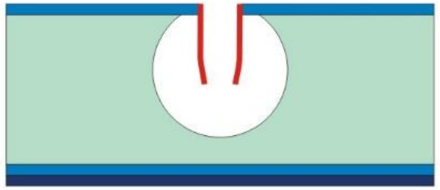
TRENCHES PASSIVATION



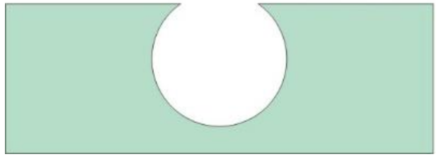
RIE ETCH-BACK ETCHING



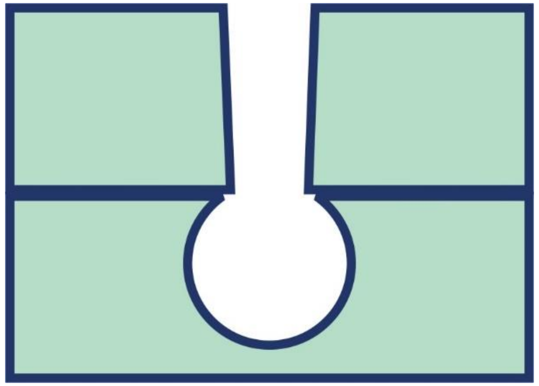
ICP ISOTROPIC ETCHING (1)



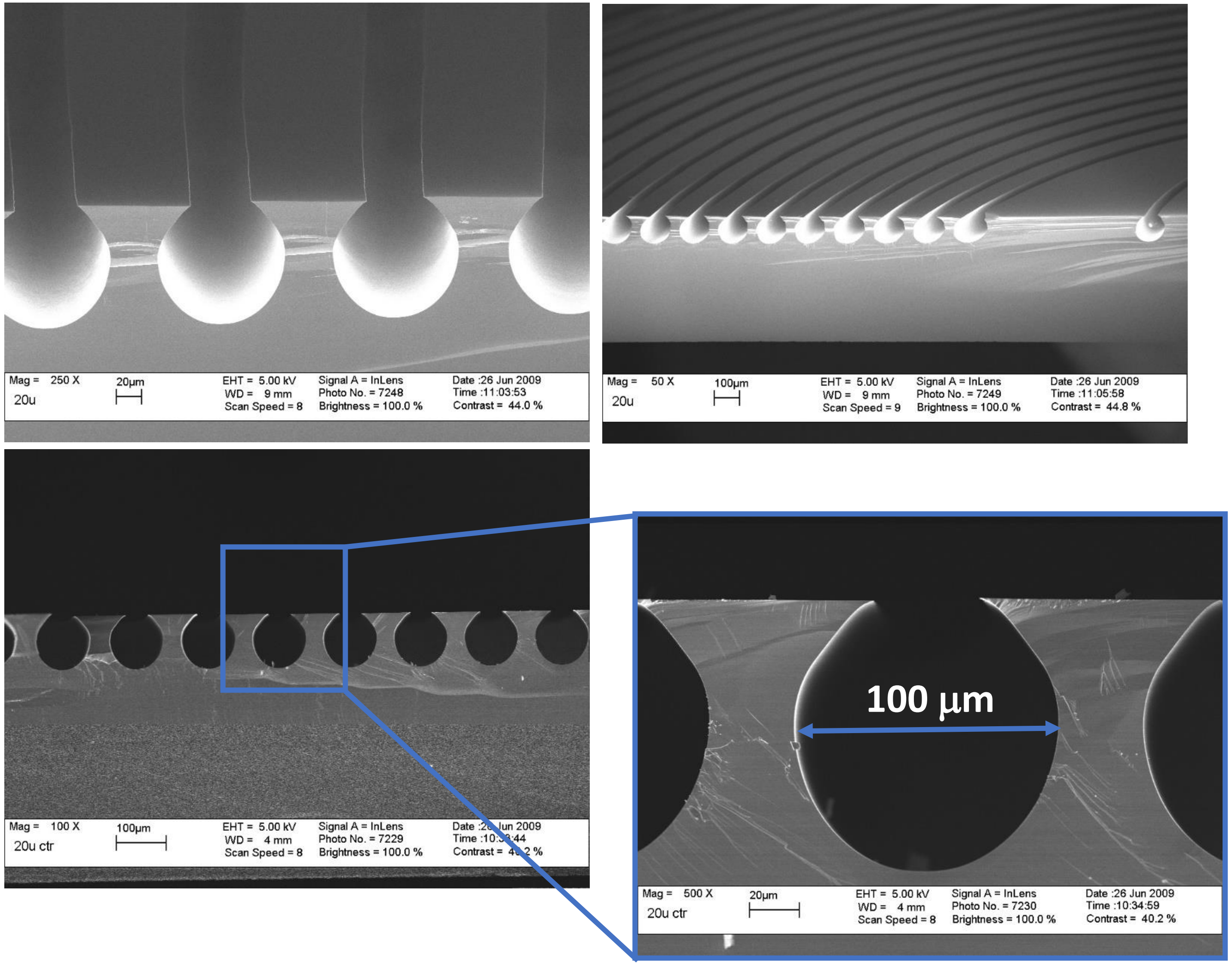
ICP ISOTROPIC ETCHING (2)



HARD MASK ETCHING



FUSION BONDING


Mag = 250 X
20u
20µm
EHT = 5.00 kV
WD = 9 mm
Scan Speed = 8
Signal A = InLens
Photo No. = 7248
Brightness = 100.0 %
Date :26 Jun 2009
Time :11:03:53
Contrast = 44.0 %
Mag = 50 X
20u
100µm
EHT = 5.00 kV
WD = 9 mm
Scan Speed = 9
Signal A = InLens
Photo No. = 7249
Brightness = 100.0 %
Date :26 Jun 2009
Time :11:05:58
Contrast = 44.8 %
Mag = 100 X
20u ctr
100µm
EHT = 5.00 kV
WD = 4 mm
Scan Speed = 8
Signal A = InLens
Photo No. = 7229
Brightness = 100.0 %
100 µm
Mag = 500 X
20u ctr
20µm
EHT = 5.00 kV
WD = 4 mm
Scan Speed = 8
Signal A = InLens
Photo No. = 7230
Brightness = 100.0 %
Date :26 Jun 2009
Time :10:34:59
Contrast = 40.2 %

THANK YOU FOR YOUR ATTENTION